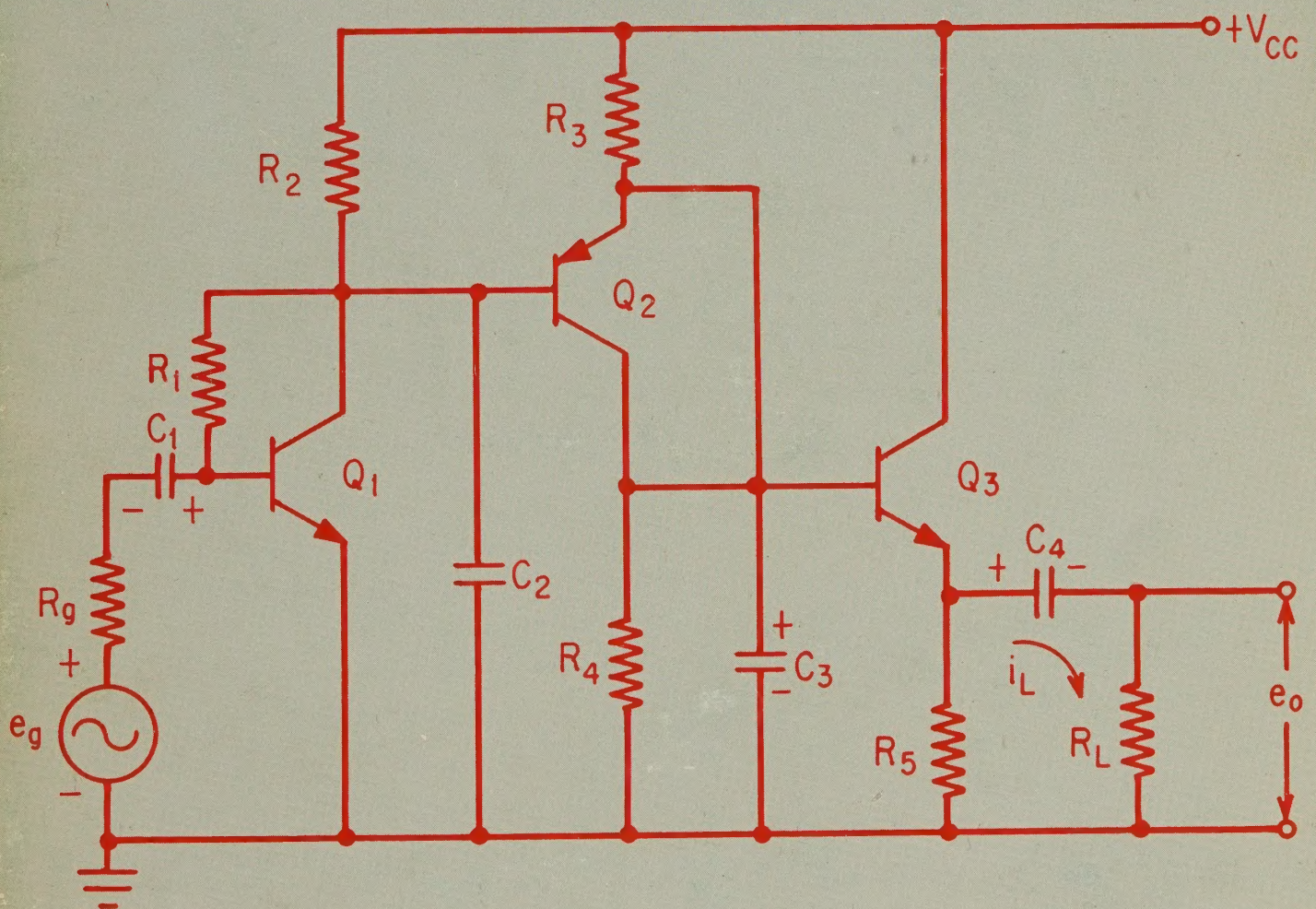


modern electronic circuit design

JAMES D. LONG



McGRAW-HILL BOOK COMPANY

modern electronic circuit design

By James D. Long

Chief Engineer

General Technology Corporation

The quickest route to a basic mastery of electronic circuit design is now yours in this one, easily understood volume. In a simple, yet exceptionally lucid fashion you are introduced to standard circuit theory. Step by step you are shown the exact procedures in planning effective and efficient electronic circuits. From analysis to design, the practical application of circuit theory is stressed, and nearly every design procedure is illustrated by a worked-out example of a typical on-the-job problem. You can use these instructive examples as models for your own design problems, or as tools to teach yourself correct design procedures.

Moving from basic circuit theory to complex applications, this book covers waveform analysis, including Fourier methods; passive circuits; equivalent circuits for tubes and semiconductors; operating point stabilization; AC amplifiers; DC amplifiers; and switching circuits such as the Schmitt, trigger, multivibrators, and the transistor inverter. It includes both vacuum-tube and transistorized circuits, and provides only the most relevant and up-to-date information for circuit designers.

Of special importance is a section that serves as a reference on components that are commercially available, and describes how the various component parameters differ. Covered here are resistors, capacitors, inductors, relays, transformers, and semiconductor diodes. In addition, there is a discussion of transistor device limitations as associated with

(continued on back flap)



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Chief Engineer

General Technology Corporation

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New York

San Francisco

Toronto

London

Sydney

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PREFACE

This book is written for those individuals who would design circuits as an occupation. It is also written for graduate engineers who have discovered in industry that there is a difference between circuit analysis and circuit design. In analyzing a given circuit, one need only apply well-established circuit principles to obtain rather definite answers. However, to design a circuit to satisfy stated requirements, one must apply judgment and creative talent because possible solutions are multiple. Seldom are there unique "right" answers to design problems; there are instead a family of acceptable answers. In some cases, even optimum answers may not exist, and, therefore, judgment is necessary. *Compromise* may possibly be the best single word to describe the process of circuit design.

Circuit analysis is fundamental to circuit design. Hence, the first few chapters are devoted to basic principles, but the emphasis and viewpoint are always directed toward the peculiar requirements of the Circuit Designer. That is, concepts and equations are developed for ready application to common design problems. Furthermore, numerous examples are included. There are, in addition, ten design examples which are completely solved to illustrate design procedure. Problems at the end of each chapter are devised to impress the student with important engineering points, and the requirement for numerous algebraic manipulations is avoided. Closed-loop operation is necessary to the learning process. Hence, answers are given to all problems. Typical or acceptable answers are given for design problems for which unique solutions are not possible.

Approximate equations are developed, where applicable, and applied to examples. The results are compared to those

obtained from complete equations so that accuracy can be determined. Many of the circuits were constructed and tested. Thus, experimental results are also available for comparison.

The treatment and presentation given to even the fundamental material differs from the customary because Circuit Designers tend to view theory from a slightly different position, i.e., from the application standpoint. For instance, worst-case analysis is covered (though only lightly) as a subject entity. But since such analysis is implicit in any circuit design which must satisfy mass production requirements, the subject of worst-case analysis is actually considered from cover to cover.

An assertion is made here that anyone who understands and is completely familiar with the contents of this book is capable of designing respectable circuits. However, practicing circuit design engineers usually find that there are also certain other rather important factors such as aptitude, experience, and knowledge of component types and characteristics. Being familiar with what is commercially available is considered so important that a complete chapter is devoted to the subject of components. Even so, this is insufficient because of the multitude of different component types. Additionally, the list of transistor types and integrated circuits is lengthy. But at least the subject is considered.

This book can be used as the basis for a course in either circuit analysis or circuit design. However, calculus is recommended as a prerequisite, although it could be taken concurrently.

JAMES D. LONG

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MODERN ELECTRONIC CIRCUIT DESIGN

FUNDAMENTALS

1-1 INTRODUCTION

The critical test for an engineer is in the application of what he knows. Every engineer possesses considerable technical knowledge, but he is capable of applying only a fraction of his knowledge to practical engineering problems. To design a circuit is to create in the sense that something comes into being which did not exist before the designer completed his work. Creation implies more than a search through literature to find a circuit with the desired characteristics. It is the application of an individual's knowledge to produce a unique result. This does not mean that the Circuit Designer is required to create continuously. He is obligated, in fact, to refrain from re-inventing the wheel. Standard circuits are standard because time and use have proved them to be satisfactory, and the Circuit Designer will usually have a good reason for deviating from proven circuits.

A vast amount of information, even in the single area of Circuit Design, is available in printed form, and much of this information must be mastered because one does not know what may be required in the future. A pertinent question is, how much material should be presented in a book on Circuit Design? If the book is complete in every respect, many vital points will be buried in essentially useless information. There may be numerous ways of solving a particular problem. Although the engineer should be familiar with several methods of solution, the requirement is that he know at least one method of solving any problem of the given type.

The material contained in this chapter is fundamental to Circuit Design, and much of it should be committed to memory.

1-2 FUNDAMENTAL RELATIONSHIPS AND OHM'S LAW

The circuit of Fig. 1-1 is used to illustrate Ohm's Law. The arrow indicates the direction of conventional current, and the three parameters in the circuit are related by Eq. (1-1).

$$E = IR \text{ volts} \quad (1-1)$$

This is Ohm's Law in mathematical form where E is measured in volts, I in amperes, and R in ohms. Ohm's Law in more general terms is indicated by the equation $e = iZ$. (It is customary to use lowercase letters for time-variant quantities and uppercase letters for time-invariant quantities.)

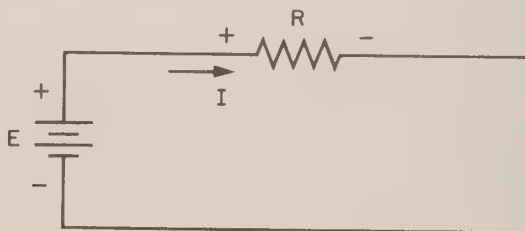


FIG. 1-1 Illustration of Ohm's Law

Energy is dissipated in the circuit of Fig. 1-1. The energy required to move a charge q through a potential difference of e volts is indicated by Eq. (1-2)

$$w = eq \text{ joules} \quad (1-2)$$

Charge q is measured in coulombs and the voltage e in volts. Current is the rate of moving charge, and the relationship is expressed mathematically by Eq. (1-3)

$$i = \frac{dq}{dt} \text{ amperes} \quad (1-3)$$

One ampere is a movement of one coulomb per second. Power is the time derivative of energy

$$p = \frac{dw}{dt} \text{ joules/sec or watts} \quad (1-4)$$

The power dissipated in the resistor in the circuit of Fig. 1-1 is found as follows:

$$\begin{aligned} p &= \frac{dw}{dt} \\ &= E \frac{dq}{dt} \\ &= EI \text{ watts} \end{aligned}$$

By Ohm's Law:

$$\begin{aligned} P &= EI \\ &= I^2 R \\ &= \frac{E^2}{R} \text{ watts} \end{aligned} \tag{1-5}$$

For instance, if the battery voltage E is 10 V, and the value of the resistor is 300 Ω , then the power dissipated in the resistor is found as follows:

$$\begin{aligned} P &= \frac{10^2}{300} \\ &= \frac{1}{3} \text{ watt} \end{aligned}$$

Resistors are manufactured with certain standard wattage ratings such as 1/4 W, 1/2 W, 1 W, etc. One would specify at least a 1/2-W resistor where the actual dissipation is 1/3-W.

The resistance of a given resistor is generally considered to be constant with time. Resistance does vary as a function of temperature, however. This is indicated more fully in the chapter on components.

Another fundamental relationship is indicated by Eq. (1-6), which allows one to compute the resistance of any given length of conductor

$$R = \frac{\rho L}{A} \text{ ohms} \tag{1-6}$$

The conductor is assumed to be of homogeneous material with resistivity ρ and constant cross-sectional area A . The resistivity of copper at 20°C is approximately 1.72×10^{-6} ohm-cm. Any consistent set of units can be used. If resistivity is given

in ohm-cm, then the length of the conductor L must be in centimeters and the cross-sectional area of the conductor in square centimeters. The cross-sectional area of standard American Wire Gauge is usually given in circular mils where 1 circular mil is equal to 7.85×10^{-7} sq in. The resistivity of copper for this set of units is 0.679×10^{-6} ohm-in.

Example 1-1

As an example, the resistance of 1,000 feet of no. 18 gauge wire is found:

$$\text{Area of no. 18 wire} = 1,620 \text{ cmil}$$

$$\text{Length} = 1,000 \text{ ft} = 12,000 \text{ in.}$$

$$\rho = 0.679 \times 10^{-6} \text{ in.-ohm}$$

$$R = \frac{\rho L}{A} = \frac{(0.679 \times 10^{-6}) (12,000)}{(1,620) (7.85) (10^{-7})} = 6.4 \Omega$$

As a matter of practice, one would use a handbook of tables to find the resistance of any given length of standard copper wire at an ambient temperature of 25°C . If the temperature is not 25°C , the resistance is found from Eq. (1-7)

$$R_2 = R_1 [1 + \alpha(t - 25)] \quad (1-7)$$

where R_2 is the resistance of the conductor at the temperature (t) in degrees centigrade, and R_1 is the resistance at 25°C . The resistance-temperature coefficient (α) is approximately 0.0039 for copper at 25°C .

1-3 KIRCHHOFF'S LAWS

Kirchhoff's Voltage Law states that the sum of all voltages around a closed circuit is zero. The circuit of Fig. 1-2 is used to illustrate this law.

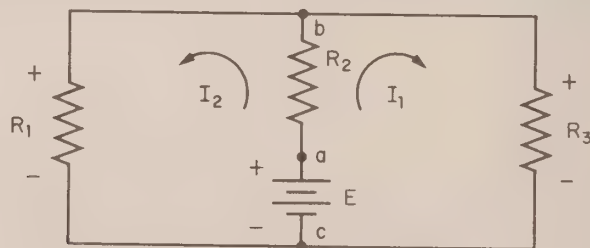


FIG. 1-2 Illustration of Kirchhoff's Voltage Law

The current I_1 conducts through a closed circuit composed of the battery E , resistor R_2 , and resistor R_3 . The current I_2 conducts through a similar closed circuit composed of the battery E , resistor R_2 , and resistor R_1 . Kirchhoff's Law states that the sum of all voltages around a closed circuit is zero

$$V_{ca} + V_{ab} + V_{bc} = 0 \quad (1-8)$$

For Eq. (1-8) to be valid, at least one of the voltages must be negative. Thus, it is clear that polarity must be established. A voltage is encountered when conventional current enters the negative pole of a battery and emerges from the positive pole. A voltage drop is encountered when current flows through a resistor as from point b to point c through resistor R_3 . The polarity of the voltage drop across resistor R_3 is as indicated by the polarity marks in Fig. 1-2.

In the double subscript notation, V_{ab} means the voltage at point a with respect to point b . In the circuit of Fig. 1-2, point a is positive with respect to point b . That is, a dc voltmeter would read upscale if the negative lead were connected to point b and the positive lead to point a . Conversely, point c is negative with respect to point a . Note also that $V_{ab} = -V_{ba}$. The voltage V_{ac} is the voltage rise of the battery. The voltage V_{ab} is the voltage drop across resistor R_2 , and V_{bc} is the voltage drop across resistor R_3 , which in this case happens to be also the voltage drop across resistor R_1 .

With the help of Kirchhoff's Current Law, a complete solution of the circuit can be obtained. This law states that the sum of all currents flowing toward a junction is zero. In other words, all the current that enters a particular junction point must also leave the point. This is analogous to pipes carrying water. In the steady state, water does not accumulate at a junction point.

Points c and b in Fig. 1-2 are junction points for the currents I_1 and I_2 . The total current flowing into point c is $I_1 + I_2$, and the only path by which this total current can leave is through the battery and resistor R_2 . Therefore, the current flowing through the battery is $I_1 + I_2$. At point b the sum current splits back into the two components I_1 and I_2 . One can now write an equation for each branch of the circuit

$$E - (I_1 + I_2)R_2 - I_1R_3 = 0$$

$$E - (I_1 + I_2)R_2 - I_2R_1 = 0$$

Generally the values of the resistors and the battery voltage are known, and the problem is to find the two branch currents I_1 and I_2 .

Example 1-2

As an example of the circuit of Fig. 1-2, let the parameter values be the following:

$$E = 10 \text{ vdc}$$

$$R_1 = 3K \text{ ohms}$$

$$R_2 = 2K \text{ ohms}$$

$$R_3 = 1K \text{ ohms}$$

To find the currents I_1 and I_2 , one writes two equations. Note that the symbol K is used to indicate multiplication by 1,000. That is, $1 K\Omega$ equals $1,000 \Omega$

$$10 - (I_1 + I_2)2K - (I_1)1K = 0$$

$$10 - (I_1 + I_2)2K - (I_2)3K = 0$$

Solving these two simultaneous equations, one gets $I_1 = 2.73 \text{ mA}$ and $I_2 = 0.91 \text{ mA}$.

It is not necessary to have chosen the proper direction for the currents I_1 and I_2 to have obtained the right answer for these currents. Indeed, in the general case, one does not know *a priori* what is the correct direction. For instance, if the current I_1 is assumed to conduct in the opposite direction to that shown in Fig. 1-2, the following equations result:

$$10 - (I_2 - I_1)2K + (I_1)1K = 0$$

$$10 - (I_2 - I_1)2K - (I_2)3K = 0$$

The solutions are $I_1 = -2.73 \text{ mA}$ and $I_2 = 0.91 \text{ mA}$. The negative sign for I_1 indicates that conduction is in a direction opposite to that chosen.

1-4 THE CAPACITOR

The capacitor is a component which exhibits certain desirable characteristics as a circuit element. Consideration of this element begins with Eq. (1-9).

$$q = Cv \text{ coul.} \quad (1-9)$$

The charge contained in a capacitor is proportional to the voltage across it, and the constant of proportionality is the magnitude of capacitance C . If one differentiates Eq. (1-9) with respect to

time (assuming that C is time invariant), Eq. (1-10) results

$$\frac{dq}{dt} = C \frac{dv}{dt} \quad \frac{\text{coul}}{\text{sec}} \quad (1-10)$$

It is known from Eq. (1-3) that $i = dq/dt$. Therefore, Eq. (1-11) follows

$$i = C \frac{dv}{dt} \quad \text{amperes} \quad (1-11)$$

The rate of change of voltage across a capacitor is proportional to the current flowing into (or out of) the capacitor. Another form of differential Eq. (1-11) is found by integration

$$v = V_o + \frac{1}{C} \int i \, dt \quad \text{volts} \quad (1-12)$$

A special case of Eq. (1-12) occurs when i is constant with time. If one assumes that the initial voltage V_o is zero, and that i is constant, then the result is Eq. (1-13)

$$v = I \frac{t}{C} \quad \text{volts} \quad (1-13)$$

This relationship is indicated by Fig. 1-3. The dotted curve illustrates the case where the initial capacitor voltage is V_o , but I and C are as before.

One can deduce from Eq. (1-12) that the voltage across a capacitor cannot be changed instantaneously if the current i is less than infinite. It is important at times in circuit design to remember that the voltage across a capacitor cannot be changed in zero time. On the other hand, very large peak currents occur when charged capacitors are shorted. Indeed, certain types of spot welders are mechanized by shorting charged capacitors into the load. The energy contained in a charged capacitor can be found from Eq. (1-14)

$$w = \frac{1}{2} C v^2 \quad \text{joules} \quad (1-14)$$

In the consideration of capacitance, some mention should be made of dielectric constant. Consider the parallel plate

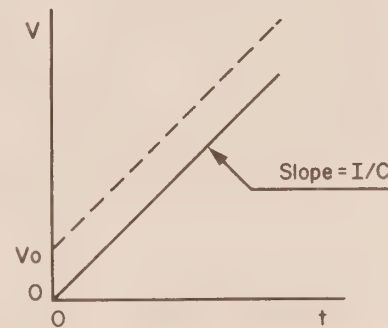


FIG. 1-3 Constant Capacitor Charging Current

capacitor of Fig. 1-4. The two plates are conductors which are separated by an insulating material such as air. Neglecting fringing effects, the capacitance is given by Eq. (1-15), where ϵ is the dielectric constant of the insulating material, A is the area of one of the plates, and d is the distance between the plates.

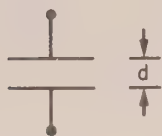


FIG. 1-4 Parallel Plate Capacitor

$$C = \epsilon \frac{A}{d} \text{ farads} \quad (1-15)$$

A consistent set of units must be used. If A is in square meters, and d is in meters, then C is in farads and ϵ is equal to 8.56×10^{-12} for vacuum or air.

Generally the relative dielectric constant K is of more interest than the dielectric constant ϵ . These quantities are related by Eq. (1-16).

$$K = \frac{\epsilon}{\epsilon_0} \quad (1-16)$$

The dielectric constant of vacuum is ϵ_0 . The relative dielectric constant of air is 1.0, polystyrene 2.6, paper 3.5, etc.

If the capacitor of Fig. 1-4 were of the air type, and if one inserted material with a relative dielectric constant of 2 between the plates, then the capacitance would be doubled. The important point to remember is that capacitance increases as the plates are brought closer together. Also, capacitance is directly proportional to the relative dielectric constant of the insulating material. A further discussion of capacitors is found in the chapter on components.

A common circuit involving a capacitor is analyzed in Example 1-3.

Example 1-3

The capacitor is initially uncharged, and the switch S_1 is closed at $t = 0$. The problem is to find the voltage across the capacitor as a function of time. One first solves for the current i as a function of time. The differential equation is:

$$E = Ri + \frac{1}{C} \int i \, dt \quad \text{volts}$$

Differentiating i with respect to t :

$$0 = R \frac{di}{dt} + \frac{i}{C}$$

$$\frac{di}{i} = \frac{-dt}{RC}$$

Integrating:

$$\ln i = \frac{-t}{RC} + k$$

$$i = \epsilon^{-t/RC}(\epsilon^k) = k_1 \epsilon^{-t/RC}$$

From initial conditions at $t = 0$, $i = E/R = k_1$.

$$i = \frac{E}{R} (\epsilon^{-t/RC})$$

$$e_0 = E - iR = E - E(\epsilon^{-t/RC})$$

$$e_0 = E(1 - \epsilon^{-t/RC}) \quad \text{volts} \quad (1-17)$$

Equation (1-17) is the solution for a step voltage input to an RC circuit of the type depicted in Fig. 1-5. This type of circuit is frequently encountered, and Eq. (1-17) should be committed to memory.

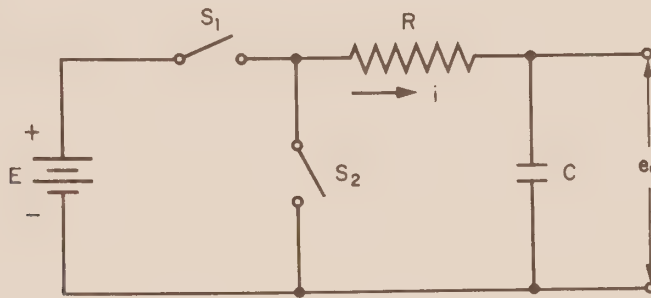


FIG. 1-5 RC Example

If after a long time switch S_1 is opened and switch S_2 is closed, the equation for the output voltage e_0 is:

$$e_0 = E \epsilon^{-t/RC} \quad \text{volts} \quad (1-18)$$

That is, the output voltage decays from the voltage E to zero volts as time t increases from zero to infinity.

1-5 THE INDUCTOR

The inductor is a circuit element which generates a voltage across it directly proportional to the rate of change of current through it. The mathematical relationship is expressed by Eq. (1-19), where the constant of proportionality is the self-inductance L in henries, e is in volts, the current i is in amperes, and t is in seconds.

$$e = L \frac{di}{dt} \text{ volts} \quad (1-19)$$

The energy stored in the magnetic field of an inductor which is conducting a current of i amperes is expressed by Eq. (1-20)

$$w = \frac{1}{2} Li^2 \text{ joules} \quad (1-20)$$

An important consideration of Eq. (1-19) is that in zero time one cannot cause a change in inductor current. If a step voltage is applied across an ideal inductor, initial current conduction is zero, but it increases from zero linearly as time increases. That is: $i = Et/L$. After a given time t , a given magnitude of current exists. If the step voltage is removed, current continues to flow until the energy in the magnetic field of the inductor has been released. If no circuit is available for the discharging current, arcing occurs between turns of the coil or across the switch contacts. Consider the circuit of Fig. 1-6.

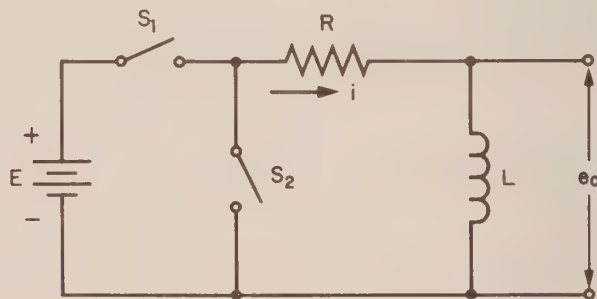


FIG. 1-6 RL Circuit

This circuit is analyzed starting with Eq. (1-21) and assuming that the switch S_1 is closed at t equals zero.

$$E = Ri + L \frac{di}{dt} \text{ volts} \quad (1-21)$$

One is usually interested in the current i as a function of time

or in the output voltage e_o as a function of time. One first solves for the current i .

$$L \frac{di}{dt} = E - Ri$$

$$\frac{di}{(E - Ri)} = \frac{dt}{L}$$

Integrating:

$$\frac{-\ln(E - Ri)}{R} = \frac{t}{L} + k_o$$

$$\ln(E - Ri) = -\frac{Rt}{L} + k$$

$$E - Ri = (\epsilon^{-Rt/L}) (\epsilon^k) = k_1 \epsilon^{-Rt/L}$$

$$i = \frac{E - k_1 \epsilon^{-Rt/L}}{R}$$

From initial conditions:

$$i = 0 \quad \text{at} \quad t = 0$$

Therefore:

$$k_1 = E$$

Hence:

$$i = \frac{E}{R} [1 - \epsilon^{-Rt/L}] \text{ amperes} \quad (1-22)$$

It is clear that the current i approaches a maximum value of E/R amperes. The output voltage e_o is found quite readily

$$e_o = E - Ri$$

$$e_o = E - \frac{RE}{R} [1 - \epsilon^{-Rt/L}]$$

$$e_o = E \epsilon^{-Rt/L} \text{ volts} \quad (1-23)$$

If after a long time switch S_1 is opened and switch S_2 is closed, the current through the inductor decays as indicated by Eq. (1-24)

$$i = I \epsilon^{-Rt/L} \text{ amperes} \quad (1-24)$$

where I equals E/R and t is measured from the time that the switches are thrown.

The resistor depicted in Fig. 1-6 may be the winding resistance of the inductor. In fact, every inductor has some winding resistance associated with it, and a quality factor Q can be defined for an inductor in terms of the resistance of the coil and the inductive reactance X_L . This relationship is indicated by Eq. (1-25)

$$Q = \frac{X_L}{R} \quad (1-25)$$

where Q is the quality factor of the inductor, R is the coil resistance in ohms, and X_L is the inductive reactance in ohms. Note that $X_L = \omega L = 2\pi fL$. Therefore, the Q of an inductor is directly proportional to frequency.

1-6 THÉVENIN'S THEOREM

Equivalent circuits and network simplification theorems are indispensable to the Circuit Designer. The characteristics of all the various components (resistors, capacitors, inductors, transistors, etc.) are expressed mathematically because circuits are designed on paper with the aid of a mathematical model. Indeed, a physical component would be useless if the mathematical relationships of that component to voltage, current, etc. were not known. An active device, such as a transistor, is reduced to an equivalent circuit of resistors, capacitors, and voltage (or current) generators. This is done because the circuit characteristics of these elements are easily expressed in convenient mathematical form. It should be recognized that equivalent circuits are not always equivalent in every respect to the actual circuit or component. For instance, the transistor is not a linear device, yet the customary equivalent circuit is linear. The more exact that one makes the equivalent circuit, the more difficult are the equations which describe it. A compromise is made between an exact mathematical model and ease of solution of the model. In other words, an inexact equivalent circuit can be quite satisfactory for the particular purposes of a Circuit Designer.

Thévenin's Theorem is used to reduce complicated circuits to more simple equivalent circuits. The equivalence of interest is at the output terminals. The reduced equivalent circuit is not equivalent in every respect to the original circuit. For one thing, there are usually more components in the original

circuit than in the reduced one. Thévenin's Theorem is used to simplify linear bilateral circuits. Figure 1-7 is used to illustrate the theorem.

By Thévenin's Theorem, one can reduce any circuit as indicated in Fig. 1-7a to an equivalent circuit as depicted in Fig. 1-7b. The Thévenin voltage generator e_g is equal to the open-circuit voltage V_{ab} of the original circuit, and the Thévenin output impedance Z_o is equal to the open-circuit voltage V_{ab} divided by the short-circuit current which is obtained by shorting terminals a and b of the original circuit. Example 1-4 is a simple application of Thévenin's Theorem.

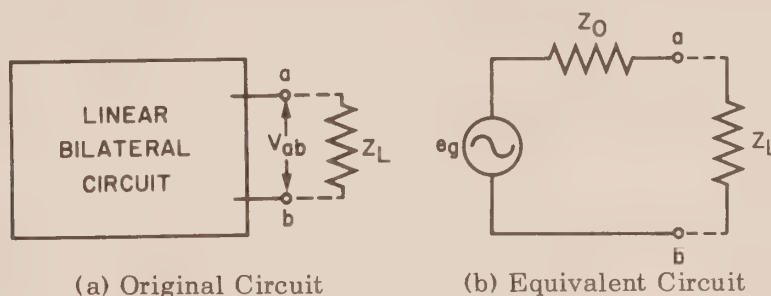


FIG. 1-7 Illustration of Thévenin's Theorem

Example 1-4

The problem is to reduce the circuit of Fig. 1-8 to a Thévenin equivalent circuit, and it is known that the equivalent circuit is of the form indicated in Fig. 1-7b.

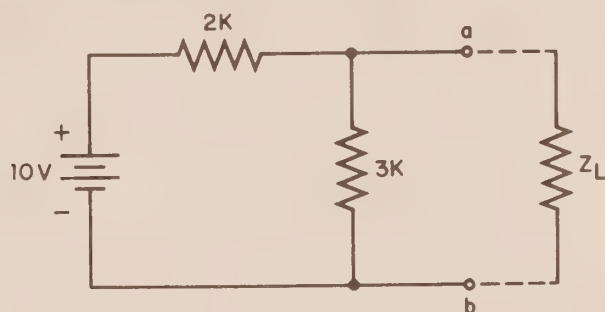


FIG. 1-8 Example of Thévenin's Theorem

The open-circuit voltage is:

$$E_{op} = \frac{(3)(10)}{2 + 3} = 6 \text{ volts}$$

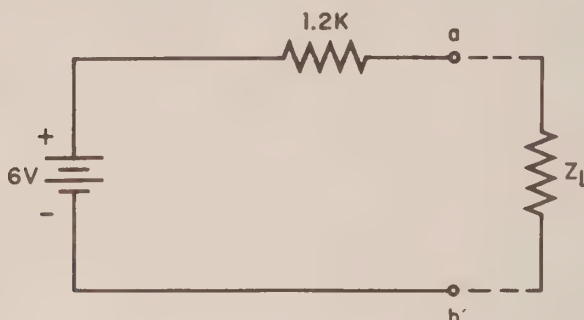
The output impedance is:

$$Z_o = \frac{E_{op}}{I_{sc}} = \frac{6}{10/2K} = 1.2 \text{ k}\Omega$$

Note also that the output impedance can be found as follows:

$$Z_o = \frac{(2)(3)K}{2 + 3} = \frac{6K}{5} = 1.2 \text{ k}\Omega$$

The following is the complete equivalent circuit.



If the terminals a and b are open, that is, if Z_L is infinite, the output voltage is 6 V. If the terminals a and b are shorted, the output current which flows through the short is 5 mA. The open-circuit voltage and the short-circuit current are the same as for the original circuit.

Straight line relationships are associated with linear circuits, and two points define a straight line. Since Thévenin's Theorem is applied to linear circuits, two points of equality between the original circuit and the equivalent circuit are sufficient to establish complete equivalence (at the output terminals). A more typical application of Thévenin's Theorem is illustrated in Example 1-5.

Example 1-5

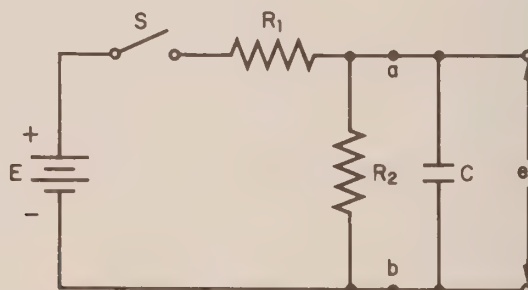


FIG. 1-9 Second Example of Thévenin's Theorem

The capacitor is initially uncharged, and the switch S is closed at t equal zero. The problem is to find the voltage across

the capacitor as a function of time. This circuit is identical to that in Example 1-4 up to the output terminals ab , and the Thévenin equivalent is found in the same way. In this case, the voltage generator magnitude and output impedance are:

$$E_T = \frac{R_2 E}{R_1 + R_2} \quad \text{and} \quad R_o = \frac{R_1 R_2}{R_1 + R_2}$$

The circuit is now reduced to the simple RC type which was solved in Example 1-3, and the result is contained in Eq. (1-17). That equation is rewritten here with the particular parameters of this problem

$$e_o = \frac{R_2 E}{R_1 + R_2} (1 - e^{-t/R_o C}) \text{ volts}$$

1-7 NORTON'S THEOREM

Norton's Theorem is virtually the same as Thévenin's Theorem except that the active element of the equivalent circuit is a current generator rather than a voltage generator. The output impedance of an ideal current generator is infinite, whereas the output impedance of an ideal voltage generator is zero ohms.

Norton's Theorem is often applied to Thévenin circuits as indicated in Fig. 1-10.

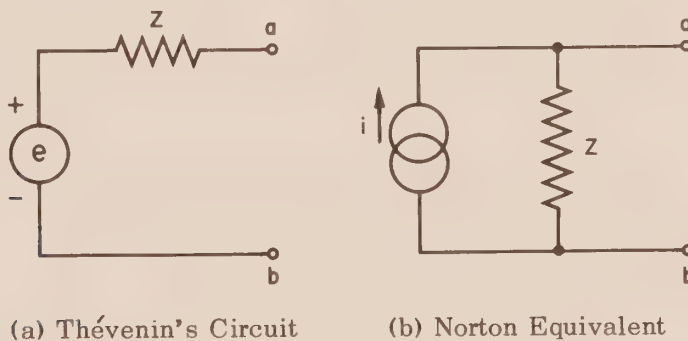


FIG. 1-10 Illustration of Norton's Theorem

In terms of the Thévenin circuit, the Norton circuit has a current generator where $i = e/Z$, and the output impedance Z is as before. The two circuits are equivalent for any load impedance connected between points a and b . An example will further illustrate the use of Norton's Theorem.

Example 1-6

The problem is to find the currents I_1 , I_2 , and I_3 by using Norton's Theorem.

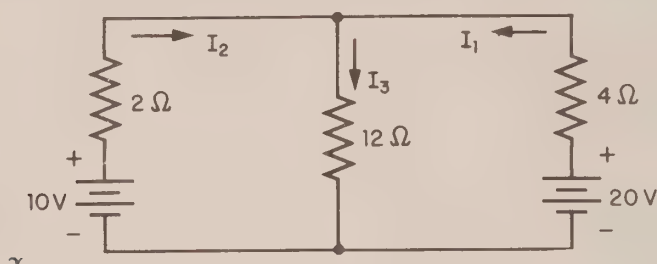
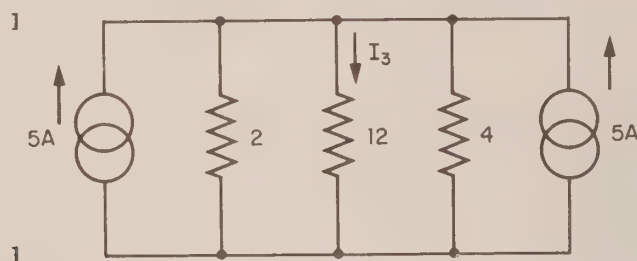
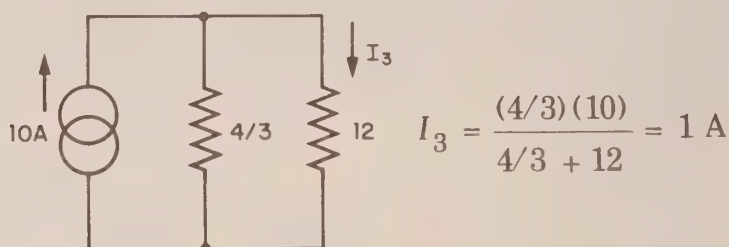


FIG. 1-11 Example of Norton's Theorem

The Norton equivalent is



The simplification continues by combining the two current generators and the 2- and 4-ohm resistors.



Since I_3 is now known, the branch currents I_1 and I_2 can be found most easily by referring to the original circuit in Fig. 1-11. The voltage across the 12-Ω resistor is:

$$E_{12} = (12)(1) = 12 \text{ volts}$$

$$I_1 = \frac{20 - 12}{4} = 2 \text{ amperes}$$

$$I_2 = \frac{10 - 12}{2} = -1 \text{ amperes}$$

The 10-V battery is being charged, and the 20-V battery is discharging.

1-8 SUPERPOSITION THEOREM

The principle of superposition is similar to the independence-of-forces law in physics. It states that, in a circuit with several voltage sources, the resultant current is the algebraic sum of the component currents which are produced by the several voltage sources. The theorem is valid only for linear circuits where the magnitudes of the elements are not a function of current. Transistors, vacuum tubes, iron core coils, etc. are examples of nonlinear elements. An example is best used to illustrate the theorem.

Example 1-7

The problem is to find the branch currents of Fig. 1-12. The procedure is to short one voltage source, find the component currents, then short the opposite voltage source and find the component currents. The result is the algebraic sum of the component currents (in each branch).

Finding the branch currents with the 6-V source shorted:

$$I_2 = \frac{12}{2 + 3/4} = 4.36 \text{ mA}$$

$$I_3 = \frac{4.36}{1 + 3} = 1.09 \text{ mA}$$

$$I_1 = \frac{(3)(4.36)}{1 + 3} = 3.27 \text{ mA}$$

Finding the branch currents with the 12-V source shorted:

$$I_1 = \frac{6}{1 + 6/5} = 2.73 \text{ mA}$$

$$I_2 = \frac{(3)(2.73)}{2 + 3} = 1.64 \text{ mA}$$

$$I_3 = \frac{(2)(2.73)}{2 + 3} = 1.09 \text{ mA}$$

The branch currents are found by adding the component currents. The direction of the currents must be noted to establish the proper sign in the summation. The directions shown in Fig. 1-12 are defined as positive. If a negative answer results for one of the currents, the assumed direction shown for that

current is incorrect. The branch currents are:

$$I_1 = -3.27 + 2.73 = -0.54 \text{ mA}$$

$$I_2 = 4.36 - 1.64 = 2.72 \text{ mA}$$

$$I_3 = 1.09 + 1.09 = 2.18 \text{ mA}$$

The 6-V battery is being charged, and the 12-V battery is discharging.

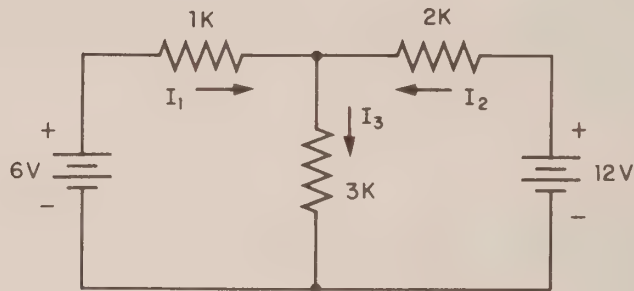


FIG. 1-12 Example of the Superposition Theorem

It should be noted that the superposition theorem is valid for ac circuits as well as dc circuits if all the elements are linear.

1-9 DESIGN EXAMPLE

In practical design assignments, there is seldom one unique “right” answer. More generally, there is a family of “right” answers. It is left to the designer’s discretion to choose a practical combination of elements to satisfy the given problem. The following design assignment is used to illustrate the point.

An output signal is required to occur in 10 ± 1 sec after the closure of a switch. The supply voltage is 30 ± 3 V, and a comparator is specified for use which will exhibit the required output signal when its input voltage is equal to 0.63 times the supply voltage (30 ± 3 V). The input impedance to the comparator is considered infinite prior to the comparison point, but the comparator draws $10 \mu\text{A}$ of input current at the comparison point. An approach to the problem is indicated in Fig. 1-13.

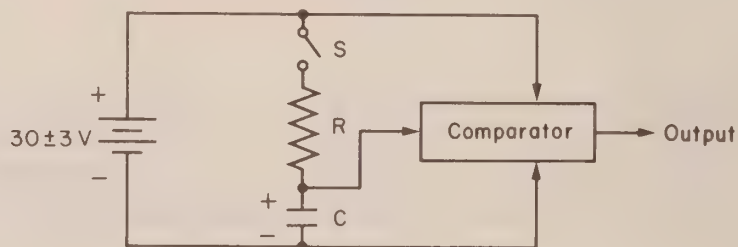


FIG. 1-13 Design Example

After the switch S is closed, the capacitor charges up to the comparison point according to Eq. (1-17). That equation is re-written here

$$e_o = E(1 - e^{-t/RC}) \text{ volts}$$

The comparison voltage e_o is defined as equal to $0.63 E$. Therefore:

$$\begin{aligned} \frac{e_o}{E} &= 0.63 = 1 - e^{-t/RC} \\ e^{-t/RC} &= 1 - .63 = 0.37 \end{aligned}$$

From tables or by using logarithms, one finds the relationship of t to RC

$$t = RC \text{ seconds}$$

The time delay required is 10 ± 1 sec. Therefore, RC equals 10 seconds. One could choose the resistor to be equal to $1 \text{ M}\Omega$ and the capacitor to $10 \text{ }\mu\text{F}$. When the capacitor has charged up to the comparison voltage, the current through the resistor will have decreased to the following value:

$$i = \frac{11}{1} = 11 \text{ }\mu\text{A}$$

Since the comparator input current at comparison is $10 \text{ }\mu\text{A}$, this solution for RC is clearly marginal. In addition, other considerations dictate the use of a tantalum-type capacitor, and leakage currents for these capacitors are not negligible. Maximum capacitor leakage current is given by the following equation:

$$I = .02CE \text{ }\mu\text{A}$$

where C is in microfarads and E is in volts. The maximum leakage current of a $10 \text{ }\mu\text{F}$ capacitor at the comparison voltage is:

$$I = (.02 \times 10 \times .63 \times 30) = 3.8 \text{ }\mu\text{A}$$

This leakage current is large in comparison to the charging current, and a different resistor-capacitor combination must be chosen.

Let the resistor equal $100 \text{ k}\Omega$ and the capacitor $100 \text{ }\mu\text{F}$. The charging current at the comparison voltage is, in this case,

110 μA . Maximum capacitor leakage current at the comparison voltage point is 38 μA . Average leakage current over the 10-sec delay period is approximately 19 μA , and the average voltage across the charging resistor is approximately 20.5 V. This leakage current could be supplied from an external resistor of the following magnitude:

$$R = \frac{20.5 \text{ V}}{19 \mu\text{A}} \simeq 1 \text{ M}\Omega$$

Instead of using two resistors in parallel, one would merely decrease the 100 K charging resistor to 91 K. (A standard 1 percent value is 90.9 K.) The tolerance specified on the time delay is ± 10 percent, so one would probably choose a tolerance for the capacitor of 5 percent and for the resistor, 1 percent.

Result:

$$R = 90.9 \text{ K } \Omega \pm 1\%$$

$$C = 100 \mu\text{F} \pm 5\%$$

It should be noted that this particular design assignment could be satisfied with an approximate resistor-capacitor combination of 200 K and 50 μF or any appropriate combination between these values and the result indicated. Size, cost, reliability, etc. would influence the designer's final choice.

PROBLEMS

- 1-1 In Fig. 1 the RC product is equal to 0.02 sec, and the capacitor is initially uncharged.

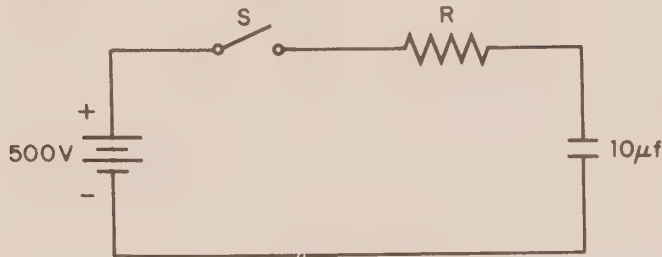


FIG. 1 RC Problem

- What is the initial current at the instant that the switch is closed?
- How much total energy will have been delivered to the circuit after a long period of time?
- How much energy will be dissipated in the resistor?

- 1-2 Solve for the current i in Fig. 2 by Kirchhoff's methods.

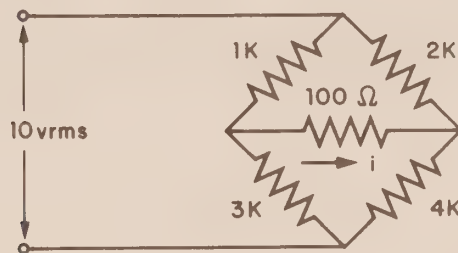


FIG. 2 Kirchhoff's Problem

- 1-3 Solve Prob. 1-2 by using Thévenin's Theorem.
Hint: Solve an equivalent circuit which contains two voltage generators and three resistors.
- 1-4 Solve for the magnitude of the voltage across the inductor in Fig. 3 by using Thévenin's Theorem.
- Note: $Z = \sqrt{R^2 + X_L^2}$

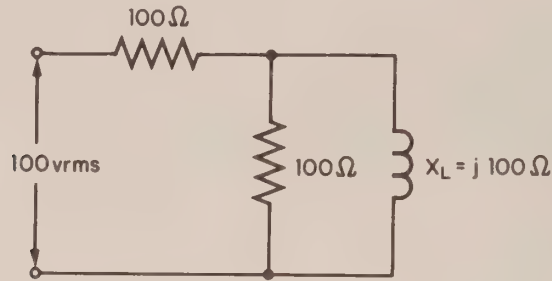


FIG. 3 Thévenin's Problem

- 1-5 a. Convert the circuit of Fig. 4 to the Norton equivalent circuit of Fig. 5, and give values for I and R .

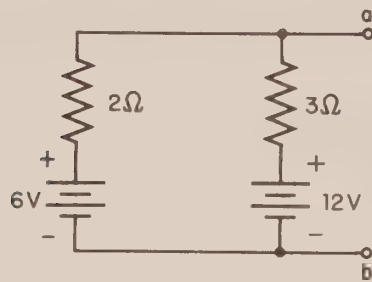


FIG. 4 Norton Problem

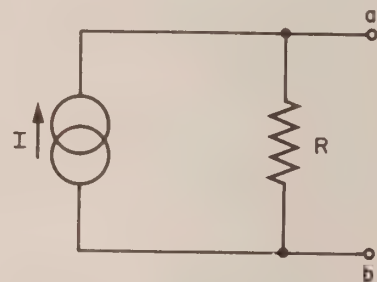


FIG. 5 Norton Equivalent

- b. Convert the circuit of Fig. 5 to the Thévenin equivalent circuit of Fig. 6, and give values for E and R .

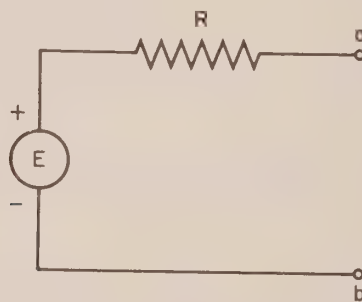


FIG. 6 Thévenin's Equivalent

- c. Prove that all three circuits are equivalent by connecting any two arbitrary impedances across the output terminals ab (such as $R = 0$ and $R = \infty$).
- 1-6 The ideal current generator in Fig. 7 provides a current step of 1 mA in magnitude at t equal zero.

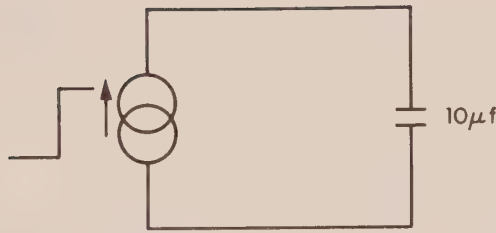


FIG. 7 Constant Current Problem

- a. What will be the voltage across the capacitor after 2 sec if it is initially uncharged?
- b. What will be the voltage across the capacitor after 2 sec if it is initially charged to 50 volts?
- c. Would any finite resistance in series with the capacitor change the result of part *a* or part *b*?

1-7 Design a circuit which will have an output impedance of $1.2\text{ k}\Omega$ resistive and a transfer characteristic of $e_o/e_{in.} = 0.6$.

1-8 Design a circuit which will charge a capacitor to 50 volts in 1 sec after a switch is closed. After the capacitor voltage has reached 50 volts, the switch will open, and the capacitor must discharge to 18.4 volts in 1 sec. See Fig. 8.

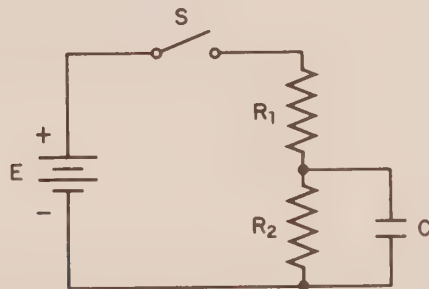


FIG. 8 Design Problem

BIBLIOGRAPHY

- Fitzgerald, A. and D. Higginbotham: "Basic Electrical Engineering," chap. 1, McGraw-Hill Book Company, New York, 1957.
- Skilling, H.: "Electrical Engineering Circuits," chap. 1, John Wiley & Sons, Inc., New York, 1957.

2

WAVEFORM ANALYSIS

2-1 THE SINE WAVE

Of all the periodic waveforms, the sine wave is the most common. Certain advantages of ac signals over dc signals are apparent, such as in the transmission of intelligence at radio frequencies. In power-distribution systems, the generated voltages are transformed up to high potential to reduce the i^2R power loss in the transmission lines. The sine wave is particularly desirable for these purposes because a single frequency is contained in an ideal sine wave whereas many frequencies are contained in a square wave, for instance. One example of the advantages inherent in the sine wave is that transformers are simpler and the transformed signal is a better reproduction of the input signal.

A characteristic of ac signals is that the signal voltage varies with time, and periodic signals vary in a mathematically definable way with time. All periodic waveforms repeat after a given period of time, and this particular time interval is called the period T of the signal. Since the output waveform from an ac signal generator varies with time, one desires to express the generator output voltage as a function of time. This is done for a sine wave in the conventional way in Eq. (2-1)

$$e = E_m \sin \omega t \text{ volts} \quad (2-1)$$

Because the voltage e is a function of time, it is often referred to as $e(t)$. If the peak voltage E_m is known, and if the angular frequency ω is known, then one can determine from Eq. (2-1) the output voltage e for any instant of time. Example

2-1 is used to illustrate the way in which the quantities in Eq. (2-1) are manipulated.

Example 2-1

A 400-cps, 26-vrms sine wave signal is to be analyzed. The period of the signal is equal to 1 over the frequency or 2.5 ms in this case. The peak voltage and the angular frequency are found as follows:

$$E_m = 26 \sqrt{2} = 36.8 \text{ volts}$$

$$\omega = 2\pi f = 2513 \text{ rad/sec}$$

The complete equation of the sine wave can now be written

$$e = 36.8 \sin 2513 t \text{ volts}$$

What is the time in seconds for the voltage e to reach a maximum of 36.8 V? This question is answered by solving the equation $\sin 2513 t = 1$. It is known that the sine of 90° is 1 and that 90° is equal to 1.57 radians. Hence:

$$2513 t = 1.57 \text{ rad}$$

$$t = 0.000625 \text{ sec} = 0.625 \text{ ms}$$

It is of interest to note that 0.625 ms is one-fourth of 2.5 ms which is the period of the waveform. An angle of 2π radians or 360° occurs during the time interval of one period, 2.5 ms in this case. It is apparent, then, that an angle of 90° occurs in 0.625 ms. The reader can verify that the voltage e will again be 36.8 V when the time $t = 0.625 + 2.5 = 3.125$ ms. One should note also that the voltage e is equal to -36.8 V when t is equal to 1.875 ms.

Engineers frequently prefer to work with degrees rather than radians. If the frequency of the signal in question is known, one can readily find the period ($T = 1/f$). The period is related to an angle of 360° , and proportions can be used to find any intermediate angle. For instance, $\sin \omega t$ is equal to $\sin 90^\circ$ at $T/4$, and $\sin \omega t$ is equal to $\sin 45^\circ$ at $T/8$, etc. There are cases where one must work with radians as with the familiar equations $X_L = \omega L$ and $X_C = 1/\omega C$. Also, the point where the response of an RC circuit is down 3 dB is defined by an equation involving ω , ($\omega = 1/RC$). The proper use of angular frequency ω , frequency f , degrees, and radians soon becomes routine with the Circuit Designer.

Frequently a relationship exists where two or more sine waves are of the same frequency, but one signal is displaced in phase from the other. This occurs in three-phase power systems, two-phase motor applications, etc. Consider the normal two-phase system where one phase is displaced by 90° from the other phase. The equations of the two signals are as follows:

$$e = E_m \sin \omega t \text{ volts}$$

$$e_1 = E_m \sin(\omega t + 90) \text{ volts}$$

With the first signal e as a reference, the second signal e_1 is leading by 90° as is indicated in Fig. 2-1. Since the angle was given as 90° , the quantity ωt must be in degrees also. If one prefers radians, then $\pi/2$ would be added to ωt instead of 90° . That is:

$$e = E_m \sin\left(\omega t + \frac{\pi}{2}\right) \text{ volts}$$

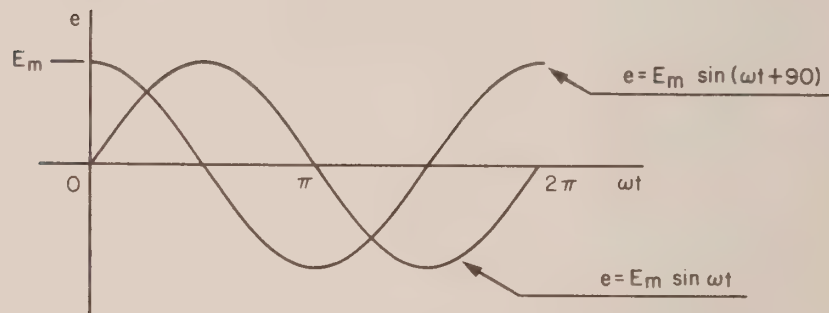


FIG. 2-1 Two-Phase Sine Waves

A more general equation is required for the general case where any phase angle may be involved. Equation (2-2) describes a sine wave with any arbitrary phase angle θ

$$e = E_m \sin(\omega t + \theta) \text{ volts} \quad (2-2)$$

Example 2-2

Two sine waves are of the same peak amplitude and frequency. At $\pi/4$ one signal is at 10 V, and the other signal is at -10 V. What is the phase angle between the two signals?

$$e_1 = 10 = E_m \sin \frac{\pi}{4} \text{ volts}$$

$$e_2 = -10 = E_m \sin\left(\frac{\pi}{4} + \theta\right) \text{ volts}$$

Dividing the two equations:

$$\begin{aligned} -1 &= \frac{\sin \pi/4}{\sin (\pi/4 + \theta)} \\ \sin \left(\frac{\pi}{4} + \theta \right) &= -.707 \\ \left(\frac{\pi}{4} + \theta \right) &= \sin^{-1}(-.707) \\ \theta &= -\frac{\pi}{2} \end{aligned}$$

The peak voltage is:

$$E_m = \frac{10}{\sin \pi/4} = 14.1 \text{ volts}$$

The two signals are defined by the following equations:

$$\begin{aligned} e_1 &= 14.1 \sin \omega t \text{ volts} \\ e_2 &= 14.1 \sin \left(\omega t - \frac{\pi}{2} \right) \text{ volts} \end{aligned}$$

Note: Since sinusoidal signals are double valued, another answer is $\theta = \pi$.

2-2 THE SQUARE WAVE

Digital Computers are constructed to operate, in general, with nonsinusoidal signals. The square wave is frequently encountered as the output signal from flip-flop counters, registers, etc. The dc-to-dc converter is another common application of the square wave where efficiency and power losses are pertinent considerations.

Two equations are used to define the square wave of Fig. 2-2. The two equations are:

$$\begin{aligned} e &= E_m \quad \text{for } 0 < \omega t < \pi \text{ volts} \\ e &= -E_m \quad \text{for } \pi < \omega t < 2\pi \text{ volts} \end{aligned} \tag{2-3}$$

Only two states are involved with the ideal square wave. That is, the voltage e is either E_m or $-E_m$ for any time t .

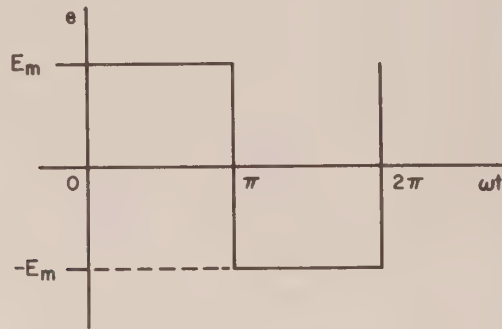


FIG. 2-2 The Square Wave

Practical square waves deviate from the ideal but usually not enough to prohibit the use of Eq. (2-3). The shape of a particular square wave depends upon how it was generated. Two typical square waves are indicated in Fig. 2-3.

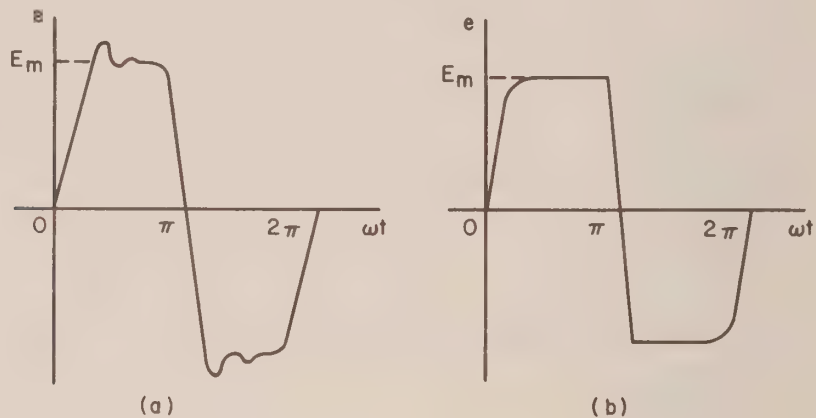


FIG. 2-3 Typical Square Waves

Variations from the ideal waveform include finite rise time, overshoot and ringing, and droop. The waveform of Fig. 2-3a often occurs where transformers are used to couple the signal to other circuits. The output signal of an astable multivibrator frequently is of the shape depicted in Fig. 2-3b. Rise time is measured from $0.1 E_m$ to $0.9 E_m$, overshoot is the amount that the signal exceeds E_m , and droop occurs when the flat portion of the curve has a negative slope with respect to the ωt axis.

Amplifier bandwidth requirements for faithful reproduction of a square wave signal of period T are more stringent than they are for a sine wave signal of the same period. This is so because many frequencies of higher order than the fundamental are contained in the square wave. The effective value and the frequency content of square waves are examined in more detail later in this chapter.

2-3 THE SAWTOOTH WAVE

It is desirable for certain applications to generate a voltage which increases linearly with time. In other words, a voltage analog for time is required where a given increment of voltage occurs for each given increment of change in time. Consider the equation for a sine wave:

$$e = E_m \sin \omega t$$

The voltage e varies as a function of time, and if one should desire to view this signal on an oscilloscope trace, a transformation must be made because the oscilloscope trace is driven by voltages rather than by time directly.

The horizontal deflection amplifier in the oscilloscope is driven from a sawtooth waveform. A characteristic sawtooth signal is indicated in Fig. 2-4. Equation (2-4) describes this signal.

$$e = \frac{(E_m)(\omega t)}{\pi} \quad \text{volts for} \quad -\pi < \omega t < \pi \quad (2-4)$$

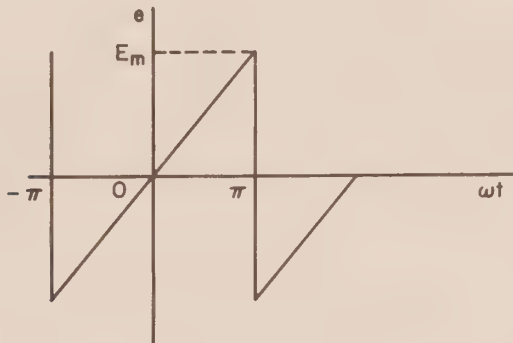


FIG. 2-4 The Sawtooth Waveform

It is readily apparent that the voltage e in Eq. (2-4) is linearly related to time. Thus, the spot on the face of an oscilloscope CRT is deflected horizontally at a constant rate of k centimeters per second. If the sine wave voltage e is connected to the vertical deflection channel in the oscilloscope, the resultant trace is that of a sine wave. Obviously, any voltage which is a function of time can also be viewed because the appropriate transformation of voltage for time is accomplished internally in the oscilloscope by using a sawtooth signal to drive the horizontal deflection amplifier.

There are some nonlinearities in a practical sawtooth waveform, and the flyback or retrace time is finite. Many

frequencies are contained in the sawtooth signal, and more analysis is required before one will properly understand this important waveform. Further consideration of the sawtooth is contained later in this chapter.

2-4 POWER

Power is important for many reasons. There is a relationship between power and energy (Eq. 1-4), between power and progress, and between power and money. From a Circuit Designer's standpoint, power is associated with efficiency, heat, resistor wattage ratings, battery current drain, amplifier design, etc.

In Chap. 1, power was defined as the time derivative of energy (Eq. 1-4). Alternately, power is defined as the rate of doing work. In a circuit consisting of resistors and batteries, power consumption is constant, and the relationships of interest are indicated in Eq. (1-5).

$$P = EI = I^2R = \frac{E^2}{R} \text{ watts} \quad (1-5)$$

Where ac signals are involved, power consumption is a function of time. Consider the curve of instantaneous power in Fig. 2-5. The equation of the curve is found quite readily assuming that the ac voltage and the resulting ac current are

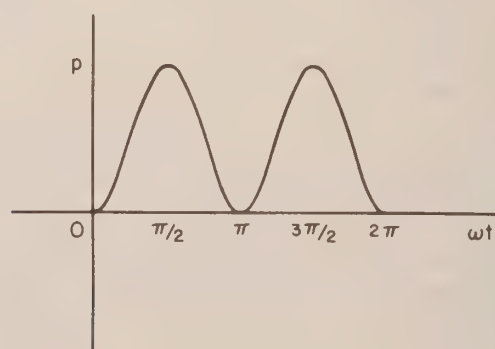


FIG. 2-5 Power

sinusoidal and in phase. Instantaneous power is equal to the instantaneous voltage multiplied by the instantaneous current.

$$p = ei = (E_m \sin \omega t) (I_m \sin \omega t) \text{ watts}$$

$$p = E_m I_m \sin^2 \omega t = P_m \sin^2 \omega t \text{ watts} \quad (2-5)$$

Peak instantaneous power is of interest at times, but more frequently one is concerned with average power. Given the equation of instantaneous power, the methods of calculus are used to find average power

$$P_{av} = \frac{1}{2\pi} \int_0^{2\pi} P_m \sin^2 \omega t \, d\omega t = \frac{P_m}{2}$$

$$P_{av} = \frac{P_m}{2} = \frac{(E_m)(I_m)}{2} \text{ watts} \quad (2-6)$$

Equations (2-5) and (2-6) apply to the circuit of Fig. 2-6.

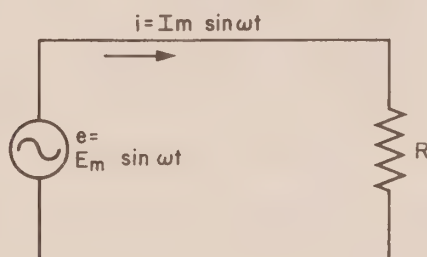


FIG. 2-6 Instantaneous Power

Peak power dissipated in the resistor is given by Eq. (2-5):

$$P_m = (E_m)(I_m) = E_m \left(\frac{E_m}{R} \right) = \frac{E_m^2}{R} \text{ watts}$$

Average power dissipated in the resistor is given by Eq. (2-6):

$$P_{av} = \frac{P_m}{2} = \frac{E_m^2}{2R} = \frac{I_m^2 R}{2} \text{ watts}$$

Two important points are noted here. Equations (2-5) and (2-6) can be used directly only if the phase angle between the current and the voltage is zero, and general usage is with root mean square (rms) rather than peak values. However, it is of fundamental importance to find average power from an equation for instantaneous power, and this point should not be neglected.

The voltage generator in Fig. 2-6 delivers a given amount of average power to the resistor. What would be the magnitude of a dc generator or battery voltage which would deliver the same average power to the same resistor? That is, what battery voltage is required to do the same work or cause the same amount of heat to be generated in the resistor? In the case of

the dc voltage, power is equal to the square of the voltage divided by the resistance R . In the case of the ac voltage, power is equal to the square of E_m divided by twice the resistance. The relationship between the battery voltage and the ac generator voltage, where both are delivering the same power, is found as follows

$$\frac{E^2}{R} = \frac{E_m^2}{2R}$$

$$E_{\text{rms}} = \frac{E_m}{\sqrt{2}} \text{ volts} \quad (2-7)$$

The equivalent or effective value of a sine wave voltage is referred to as E_{rms} and is related to the peak value of the sine wave voltage as indicated by Eq. (2-7).

An ac voltage of magnitude 115 vrms would deliver the same power to a $10\text{-}\Omega$ resistor, for instance, as would 115 vdc. If the ac voltage were sinusoidal, the peak voltage would be $115\sqrt{2}$ volts.

The relationship of the effective or rms value of a sinusoidal voltage to the peak value was found rather simply, and further analysis would not necessarily be required were it not for other waveforms such as square waves, sawtooth waves, etc. Unfortunately, Eq. (2-7) is not valid for any waveform except sinusoidal waveforms. It is a special solution of a more general equation and is particularly important because sinusoidal waveforms are quite common. Equation (2-8) is applicable to any periodic waveform.

$$(E_{\text{rms}})^2 = \frac{1}{2\pi} \int_0^{2\pi} e^2 d\omega t \text{ (volts)}^2 \quad (2-8)$$

Example 2-3

The rms value of a sine wave is derived in terms of the peak value by using Eq. (2-8). The peak value is involved because the equation for a sine wave is written in terms of peak voltage.

$$e = E_m \sin \omega t \text{ volts}$$

$$(E_{\text{rms}})^2 = \frac{1}{2\pi} \int_0^{2\pi} (E_m \sin \omega t)^2 d\omega t$$

$$E_{\text{rms}} = \frac{E_m}{\sqrt{2}} \text{ volts}$$

It is of interest to note that the rms voltage of a waveform is independent of frequency.

Example 2-4

The rms value of a square wave is found by using Eq. (2-8)

$$e = E_m \quad \text{for} \quad 0 < \omega t < \pi \quad [\text{See Eq. (2-3)}]$$

Since the waveform is symmetrical, the rms value can be found by integrating from zero to π

$$(E_{\text{rms}})^2 = \frac{1}{\pi} \int_0^{\pi} (E_m)^2 d\omega t = \frac{\pi(E_m)^2}{\pi}$$

$$E_{\text{rms}} = E_m \quad \text{volts}$$

The rms value of a square wave is equal to the peak value.

In certain cases, standard waveforms may be added to a dc bias or offset voltage. Consider a sine wave with a dc bias

$$e = 2 + 3 \sin \omega t \quad \text{volts}$$

Equation (2-8) can be used to find the rms value, but an easier method is applicable since the rms value of a sine wave, in relation to the peak value, is known

$$(E_{\text{rms}})^2 = (2)^2 + \left(\frac{3}{\sqrt{2}} \right)^2 = 8.5$$

$$E_{\text{rms}} = \sqrt{8.5} \quad \text{volts}$$

This method is generalized by Eq. (2-9)

$$E_{\text{rms}} = \sqrt{(E_{\text{dc}})^2 + (E_{\text{rms}})_1^2 + (E_{\text{rms}})_2^2 + \cdots + (E_{\text{rms}})_n^2} \quad (2-9)$$

Example 2-5

Find the average value of the waveform in Fig. 2-7 and the rms value. The average value is found quite readily as follows:

$$E_{\text{av}} = \frac{3 \times 2 + 1 \times 1}{3} = \frac{7}{3} \quad \text{volts}$$

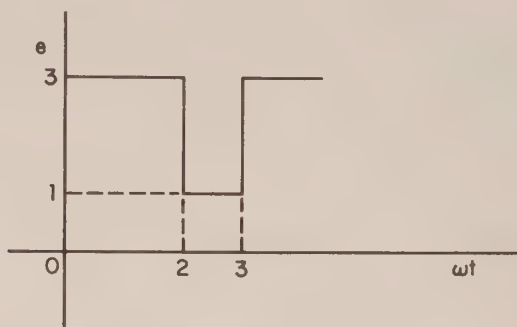


FIG. 2-7 RMS Voltage

The rms value is calculated as follows:

$$(E_{\text{rms}})^2 = \frac{3^2 \times 2 + 1^2 \times 1}{3} = \frac{19}{3}$$

$$E_{\text{rms}} = \sqrt{6.33} \text{ volts}$$

Waveforms of current instead of voltage are analyzed in the same way. That is, Eq. (2-8) is applicable to problems involving rms currents if the voltage terms are replaced by current terms.

The average value of a sine wave (or square wave) is zero. However, it is common practice in the design of power supplies to half-wave or full-wave-rectify sinusoidal voltages. The average or dc value of the rectified waveform is of interest. Consider the full-wave rectified signal in Fig. 2-8.

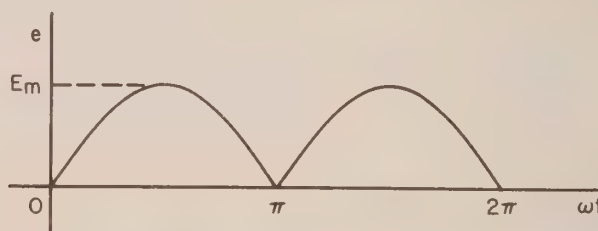


FIG. 2-8 Full-Wave Rectified Sine Wave

The equation of this signal in the interval from 0 to π is:

$$e = E_m \sin \omega t \text{ volts}$$

As in the case of average power, the methods of calculus are used to find the average value of this waveform

$$E_{\text{av}} = \frac{1}{\pi} \int_0^{\pi} E_m \sin \omega t d\omega t$$

$$E_{\text{av}} = \frac{2E_m}{\pi} = 0.637 E_m \text{ volts} \quad (2-10)$$

Equation (2-10) indicates the relationship between the peak value of a sine wave and the full-wave-rectified average value. The Circuit Designer will know this relationship from memory. The student can verify that the average value of a full-wave-rectified square wave is equal to the peak value which in turn is equal to the rms value.

One should note that the peak value of a waveform is not at all the same as the peak-to-peak value, the latter being twice the former for symmetrical waveforms.

The average power which is consumed in the circuit of Fig. 2-6 is defined by Eq. (2-6) in terms of E_m and I_m . Average power can now be defined in terms of E_{rms} and I_{rms}

$$P_{\text{av}} = \frac{E_m I_m}{2} = \left(\frac{E_m}{\sqrt{2}} \right) \left(\frac{I_m}{\sqrt{2}} \right) = E_{\text{rms}} I_{\text{rms}} \text{ watts}$$

Because rms values are frequently used, it is standard practice to write an rms voltage (or current) as E (or I) rather than E_{rms} (or I_{rms}). Subscripts are used to refer to peak values or average values such as E_m , E_{max} , E_{pk} , or E_{av} .

One condition of interest still exists, and that is the case where there is a phase angle between current and voltage. This case is illustrated with the two following equations:

$$e = E_m \sin \omega t \text{ volts}$$

$$i = I_m \sin (\omega t + \theta) \text{ amperes}$$

The equation for instantaneous power is found by multiplying the equation for instantaneous voltage by the corresponding equation for current.

$$p = ei = E_m I_m (\sin \omega t) (\sin \omega t + \theta)$$

By using a trigonometric identity and eliminating terms which are zero, average power is found.

$$\begin{aligned} P_{\text{av}} &= \frac{E_m I_m \cos \theta}{2\pi} \int_0^{2\pi} \sin^2 \omega t \, d\omega t \\ &= \frac{E_m I_m \cos \theta}{2} = E_{\text{rms}} I_{\text{rms}} \cos \theta \end{aligned}$$

$$P = EI \cos \theta \text{ watts} \quad (2-11)$$

Average power is the product of the rms voltage, the rms current, and the cosine of the phase angle. Power factor is another term for $\cos \theta$ when Eq. (2-11) is used.

2-5 FOURIER METHODS

Any periodic waveform can be defined by a series such as Eq. (2-12).

$$e = \frac{a_0}{2} + a_1 \cos \theta + a_2 \cos 2\theta + \cdots + a_n \cos n\theta + b_1 \sin \theta + b_2 \sin 2\theta + \cdots + b_n \sin n\theta \text{ volts} \quad (2-12)$$

This equation is a Fourier series where:

$$a_0/2 = \text{Average value or dc component}$$

$$\theta = \omega t$$

$$a_n = \frac{1}{\pi} \int_0^{2\pi} f(\theta) \cos n\theta \, d\theta \quad (2-13)$$

$$b_n = \frac{1}{\pi} \int_0^{2\pi} f(\theta) \sin n\theta \, d\theta \quad (2-14)$$

Consideration is given to Eq. (2-12) because it is a powerful tool to the Circuit Designer. The square wave was defined by Eq. (2-3), but the information contained therein is insufficient for many purposes. Suppose that an amplifier is to be designed where the input signal is a square wave of a given repetition frequency. What amplifier bandwidth is required to reproduce the square wave? Although Eq. (2-3) defines the square wave, it does not answer the bandwidth question. It will soon be apparent that the upper cutoff frequency of the amplifier must be considerably greater than the square wave repetition frequency if the waveform is to be faithfully reproduced.

It is possible to write another equation for a square wave other than Eq. (2-3) which contains the desired frequency information. The Fourier series is used to derive the required equation of the square wave which is depicted in Fig. 2-2. The task is to evaluate the a and b coefficients for use with Eq.

(2-12). The a coefficients are found from Eq. (2-13) as follows:

$$a_n = \frac{1}{\pi} \int_0^{2\pi} f(\theta) \cos n\theta d\theta$$

$$a_n = \frac{1}{\pi} \left[\int_0^{\pi} E_m \cos n\theta d\theta + \int_{\pi}^{2\pi} -E_m \cos n\theta d\theta \right]$$

$$a_n = \left[\frac{E_m \sin n\theta}{n\pi} \right]_0^{\pi} - \left[\frac{E_m \sin n\theta}{n\pi} \right]_{\pi}^{2\pi}$$

$$a_n = 0$$

It is obvious that all the a coefficients are zero for any integral value of n except possibly for the case where n equals zero. However, it is known that $a_0/2$ is the dc component of the waveform, and the dc component is zero for the waveform under consideration. Hence, all the a coefficients are zero.

The b coefficients are found from Eq. (2-14).

$$b_n = \frac{1}{\pi} \int_0^{2\pi} f(\theta) \sin n\theta d\theta$$

$$b_n = \frac{1}{\pi} \left[\int_0^{\pi} E_m \sin n\theta d\theta + \int_{\pi}^{2\pi} -E_m \sin n\theta d\theta \right]$$

$$b_n = \left[\frac{-E_m \cos n\theta}{n\pi} \right]_0^{\pi} + \left[\frac{E_m \cos n\theta}{n\pi} \right]_{\pi}^{2\pi}$$

$$b_n = \frac{E_m}{n\pi} [1 + \cos 2n\pi - 2 \cos n\pi]$$

For all even integral values of n , b_n equals zero. For all odd values of n , b_n equals $4E_m/n\pi$. The desired equation for the square wave can now be written

$$e = \frac{4E_m}{\pi} \left(\sin \omega t + \frac{\sin 3\omega t}{3} + \frac{\sin 5\omega t}{5} + \dots \right) \text{ volts} \quad (2-15)$$

The square wave of Fig. 2-2 contains only odd harmonics which decrease in amplitude as the order of the harmonic increases. Although the series of Eq. (2-15) is theoretically infinite, one can truncate the series after a given number of terms to approximate the true square wave as accurately as desired. The important advantage of Eq. (2-15) is that one can determine the frequency content of the square wave and, therefore, amplifier bandwidth requirements.

Example 2-6

The sawtooth waveform of Fig. 2-4 is to be analyzed for frequency content. The waveform is defined by Eq. (2-4), and the task, as before, is to evaluate the a and b coefficients for application with Eq. (2-12)

$$\begin{aligned} a_n &= \frac{1}{\pi} \int_{-\pi}^{\pi} f(\theta) \cos n\theta \, d\theta \\ a_n &= \frac{1}{\pi} \int_{-\pi}^{\pi} \frac{\theta E_m}{\pi} \cos n\theta \, d\theta \\ a_n &= \frac{E_m}{\pi^2} \left[\frac{\cos n\theta}{n^2} + \frac{\theta \sin n\theta}{n} \right]_{-\pi}^{\pi} \end{aligned}$$

The a coefficients are evidently all zero except possible a_0 . However, the dc component of the waveform is zero, and therefore, all of the a coefficients are zero.

The b coefficients are found as follows:

$$\begin{aligned} b_n &= \frac{1}{\pi} \int_{-\pi}^{\pi} \frac{\theta E_m}{\pi} \sin n\theta \, d\theta \\ b_n &= \frac{E_m}{\pi^2} \left[\frac{\sin n\theta}{n^2} - \frac{\theta \cos n\theta}{n} \right]_{-\pi}^{\pi} \end{aligned}$$

$$b_n = \frac{2E_m}{n^2\pi^2} (\sin n\pi - n\pi \cos n\pi)$$

For even integers of n , $\sin n\pi = 0$ and $\cos n\pi = 1$, and $b_n = -2E_m/n\pi$. For odd integers of n , $\sin n\pi = 0$ and $\cos n\pi = -1$, and $b_n = 2E_m/n\pi$.

The desired equation for the sawtooth waveform can now be written [Eq. (2-16)]

$$e = \frac{2E_m}{\pi} \left[\sin \omega t - \frac{1}{2} \sin 2\omega t + \frac{1}{3} \sin 3\omega t - \cdots \right] \text{ volts} \quad (2-16)$$

Normally, the Circuit Designer will use a handbook or textbook to find the Fourier series of a given standard periodic waveform. However, there are times when the methods of this section will be used, and one will discover that the work involved will be minimized if the axes and integration limits are appropriately chosen. For instance, the a coefficients were all zero for the square wave of Fig. 2-2 because of the choice of the axes and integration limits.

Example 2-7

The frequency content of the half-wave rectified sinusoidal waveform of Fig. 2-9 is to be determined.



FIG. 2-9 Half-Wave Rectified Waveform

The equation of the waveform from $-\pi/2$ to $\pi/2$ is:

$$e = E_m \cos \omega t$$

The next step is to solve for the a coefficients

$$a_n = \frac{E_m}{\pi} \int_{-\pi/2}^{\pi/2} \cos \theta \cos n\theta d\theta$$

$$a_n = \frac{E_m}{\pi} \left[\frac{\sin(n-1)\theta}{2(n-1)} + \frac{\sin(n+1)\theta}{2(n+1)} \right]_{-\pi/2}^{\pi/2} \quad n^2 \neq 1$$

$$a_n = \frac{2E_m}{\pi} \left[\frac{\sin(n-1)\pi/2}{2(n-1)} + \frac{\sin(n+1)\pi/2}{2(n+1)} \right] \quad n^2 \neq 1$$

One solves for the coefficients by substituting $n = 0, 2, 3, 4$, etc., into the equation

$$a_0 = \frac{E_m}{\pi} (1 + 1) = \frac{2E_m}{\pi}$$

$$a_2 = \frac{E_m}{\pi} \left(1 - \frac{1}{3} \right) = \frac{2E_m}{3\pi}$$

$$a_3 = \frac{E_m}{\pi} (0 + 0) = 0$$

$$a_4 = \frac{E_m}{\pi} \left(-\frac{1}{3} + \frac{1}{5} \right) = -\frac{2E_m}{15\pi}$$

$$a_5 = \frac{E_m}{\pi} (0 + 0) = 0$$

For the case where $n = 1$, the equation for a_n is:

$$a_n = \frac{E_m}{\pi} \int_{-\pi/2}^{\pi/2} \cos^2 \theta \, d\theta$$

$$a_1 = \frac{E_m}{\pi} \left[\frac{\theta}{2} + \frac{\sin 2\theta}{4} \right]_{-\pi/2}^{\pi/2} = \frac{E_m}{2}$$

The b coefficients are found as follows:

$$b_n = \frac{E_m}{\pi} \int_{-\pi/2}^{\pi/2} \cos \theta \sin n\theta \, d\theta$$

$$b_n = \frac{-E_m}{2\pi} \left[\frac{\cos(n-1)\theta}{n-1} + \frac{\cos(n+1)\theta}{n+1} \right]_{-\pi/2}^{\pi/2} \quad n^2 \neq 1$$

$$b_n = 0$$

If $n = 1$, the solution to the integral is:

$$b_1 = \frac{E_m}{2\pi} \left(\sin^2 \theta \right)_{-\pi/2}^{\pi/2} = 0$$

Thus, all the b coefficients are zero, and the desired equation is found by substituting the nonzero coefficients into Eq. (2-12)

$$e = \frac{E_m}{\pi} \left[1 + \frac{\pi}{2} \cos \omega t + \frac{2}{3} \cos 2\omega t - \frac{2}{15} \cos 4\omega t + \dots \right] \quad (2-17)$$

The average or dc component is equal to E_m/π , and the peak value of the fundamental ripple is $E_m/2$. Also, the peak value of the second harmonic ripple voltage is two-thirds of the dc voltage. The implication is that filtering requirements for extraction of the dc component from a half-wave-rectified sinusoidal signal are rather stringent.

2-6 DESIGN EXAMPLE

A filter must be designed to extract the fundamental sine wave component from a 26-vrms, 400-cps square wave. The proposed filter is indicated in Fig. 2-10.

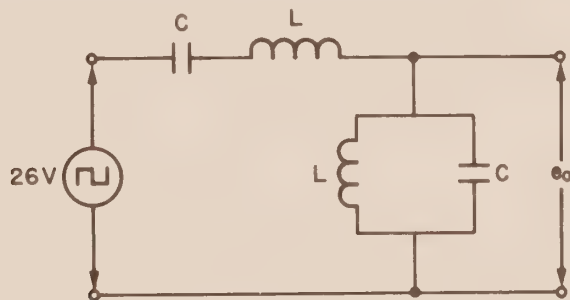


FIG. 2-10 LC Filter

Since the desired output signal is to be a 400-cps sine wave, the series and parallel circuits must be resonant to 400 cps.

$$f_0 = 400 = \frac{1}{2\pi\sqrt{LC}}$$

$$\sqrt{LC} = \frac{1}{800\pi}$$

$$LC = \frac{10^{-6}}{0.64 \pi^2} = 0.158 \times 10^{-6}$$

One can choose the inductor and solve for the capacitor. Inductors of high value are often undesirable because of size and weight restrictions. However, better filtering results are obtained if the inductive reactance and the coil Q are high. The required coil Q depends upon how much distortion is allowable in the output, but 50 can be chosen as a reasonable value. The inductive reactance of a 1-H inductor is calculated:

$$X_L = \omega L = (6.28)(400)(1) = 2.5 \text{ k}\Omega$$

The dc resistance of the coil is equal to the inductive reactance divided by the specified Q . The resulting resistance is 50Ω which is not an unusual requirement for 1-H inductors. Thus, the filter components are specified as follows:

$$L = 1 \text{ H, DCR} < 50 \Omega$$

$$C = 0.15 \mu\text{F}$$

It is known from practice that the total harmonic distortion in the output signal is approximately 5 percent for the circuit of Fig. 2-10 with the specified component values. The maximum theoretical value of the output sine wave is found from Eq. (2-15)

$$e = \left(\frac{4E_m}{\pi} \right) (\sin \omega t) = 33.1 \sin 2513 t$$

$$e = 33.1 \sin 2513 t \text{ volts}$$

The design components were specified as 1-H and $0.15 \mu\text{F}$. Quite obviously, there are other combinations which will satisfy the design assignment. The optimum values would depend upon more specific requirements such as the allowable distortion in the output waveform. For instance, if the series tuned circuit is changed to 4.8-H and $0.033 \mu\text{F}$, the total harmonic distortion will decrease to approximately 1 percent.

PROBLEMS

- 2-1 The voltage generator which is depicted in Fig. 1 produces a voltage which is expressed by the following equation:

$$e = 163 \sin 377t \text{ volts}$$

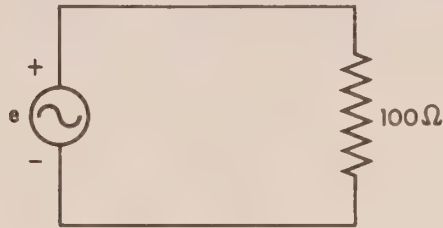


FIG. 1 Sine-Wave Voltage Generator

- a. What is the rms voltage?
 - b. How much power is dissipated in the resistor?
 - c. What is the frequency of the signal?
- 2-2 Two sine-wave voltages are expressed by the following two equations:

$$e_1 = 100 \sin 2513t \text{ volts}$$

$$e_2 = 100 \sin (2513t + \theta) \text{ volts}$$

At $t = 0$, the voltage e_1 is 0 and the voltage e_2 is -70.7 V.

- a. What is the phase angle θ ?
 - b. What is the frequency of the two signals?
 - c. What is the period of the two signals?
- 2-3 A square-wave voltage is depicted in Fig. 2 and defined by the following two equations:

$$e = 100 \text{ V} \quad \text{for} \quad \pi > \omega t > 0$$

$$e = 0 \text{ V} \quad \text{for} \quad 2\pi > \omega t > \pi$$

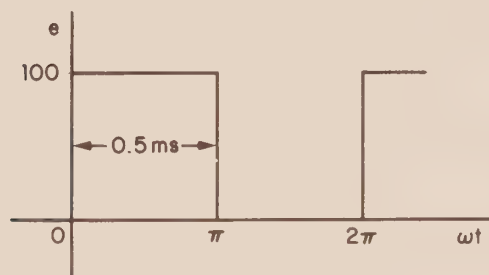


FIG. 2 Square Wave

- a. What is the dc component of the waveform?
- b. What is the rms value of the waveform?
- c. What is the repetition frequency?

2-4 Consider the circuit of Fig. 3. The voltage and current waveforms are defined by the following two equations:

$$e = 100 \sin \omega t \text{ volts}$$

$$i = 10 \sin \left(\omega t + \frac{\pi}{4} \right) \text{ amperes}$$

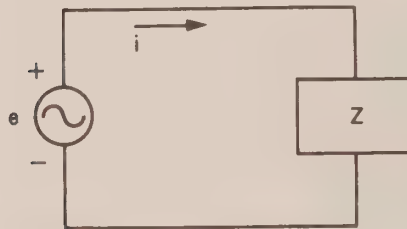


FIG. 3 Reactive Circuit

- a. What is the phase angle between current and voltage?
- b. How much power is being dissipated?
- c. How many volt-amperes are being delivered to the load Z ?
- d. What is the equation of instantaneous power?

2-5 Solve for the Fourier series of the full-wave-rectified sinusoidal signal depicted in Fig. 4.

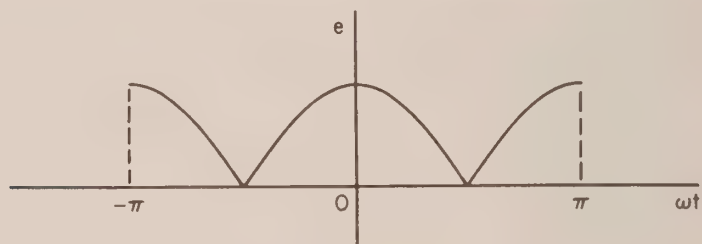


FIG. 4 Full-Wave-Rectified Waveform

The equation of the signal is:

$$e = E_m \cos \omega t \quad \frac{\pi}{2} > \omega t > \frac{-\pi}{2}$$

$$e = -E_m \cos \omega t \quad \frac{3\pi}{2} > \omega t > \frac{\pi}{2}$$

- 2-6 All the components in the circuit of Fig. 5 are considered ideal. The transformer turns ratio is 1:2 CT (1:1:1). The input voltage across resistor R_1 is 115 vrms, and the voltage across resistor R_2 is $(2)(115)(\sqrt{2})/\pi$ volts. Assume $X_L \gg R_2$ and $X_C \ll R_2$. The power dissipated in resistor R_1 is $(115)^2/R_1$, and the power dissipated in R_2 is $(8/R_2)(115/\pi)^2$.

$$P_1 = \frac{115^2}{R_1} \text{ watts}$$

$$P_2 = \frac{8}{\pi^2} \frac{115^2}{R_2} \text{ watts}$$

P_2 is less than P_1 if R_1 is equal to R_2 . Explain why this is so assuming lossless transformer, rectifiers, inductor, etc.

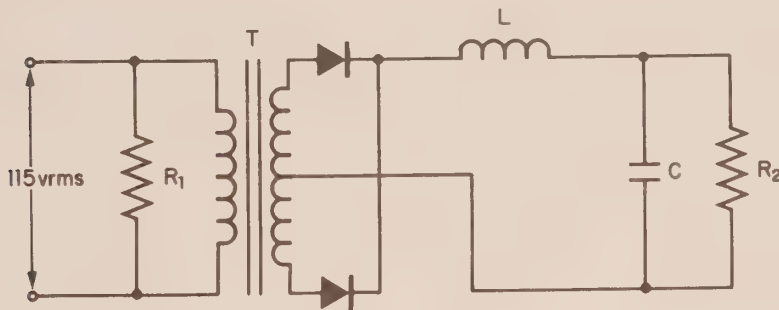


FIG. 5 Rectifier Circuit

- 2-7 Design a filter with the configuration shown in Fig. 6 which will extract the fundamental sine wave component from the signal depicted in Fig. 7. The repetition frequency of the pulse train is 1000 pps.

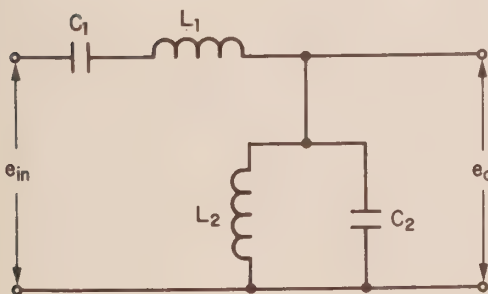


FIG. 6 Filter

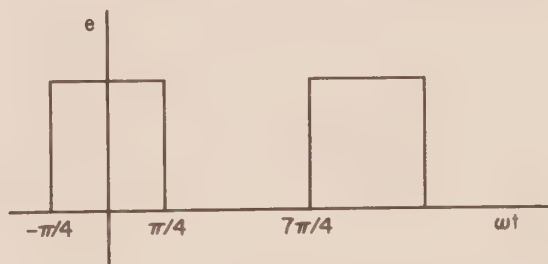


FIG. 7 Input Signal (e_{in})

The input signal is defined by the following equation:

$$e = 10 \text{ V} \quad \frac{\pi}{4} > \omega t > \frac{-\pi}{4}$$

$$e = 0 \quad \frac{7\pi}{4} > \omega t > \frac{\pi}{4}$$

What is the rms value of the filtered output voltage assuming ideal components?

- 2-8 The input voltage to the black box of Fig. 8 is defined by the equation $e = 26\sqrt{2} \sin 2513t$ volts, and the output signal is defined by the equation $e = -52\sqrt{2} \sin 2513t$ volts. Design a circuit, using ideal components, which will replace the black box.

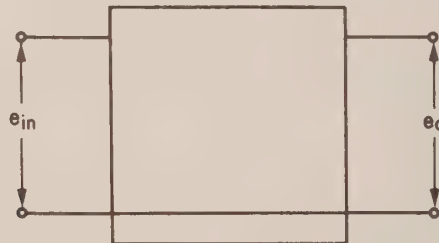


FIG. 8 Black Box

BIBLIOGRAPHY

- Moskowitz, S. and J. Racker: "Pulse Techniques," chap. 1, Prentice-Hall, Inc., New York, 1951.
 Skilling, H.: "Electrical Engineering Circuits," chap. 14, John Wiley & Sons, Inc., New York, 1957.

PASSIVE CIRCUITS

3-1 COMPLEX ALGEBRA

The engineer is confronted with the task of solving a variety of technical problems. Sometimes the required solution to a given problem is obtained empirically by performing tests on existing equipment. However, one usually desires an analytical solution which can be verified by more than one mathematical approach or by laboratory tests. Certain classes of problems are solved more easily by a particular method. In Chap. 2, for instance, the sine wave was defined by a familiar expression ($e = E_m \sin \omega t$) but this is not the only way to define a sine wave. Equation (3-1) indicates other expressions which are also mathematically valid

$$\begin{aligned}
 e &= E_m \sin \omega t = \left(\frac{e^{j\omega t} - e^{-j\omega t}}{j2} \right) E_m = \operatorname{Re} E_m \angle \omega t - \pi/2 \\
 &= \operatorname{Re} E_m \left[\cos \left(\omega t - \frac{\pi}{2} \right) + j \sin \left(\omega t - \frac{\pi}{2} \right) \right] \quad (3-1)
 \end{aligned}$$

The latter expression of Eq. (3-1) is derived from the phasor diagram that is depicted in Fig. 3-1.

The phasor of magnitude E_m rotates in a counterclockwise direction at a constant angular frequency of ω radians per second. The phasor, $E_m \angle \omega t$, can be expressed in rectangular form as follows

$$E_m \angle \omega t = E_m (\cos \omega t + j \sin \omega t)$$

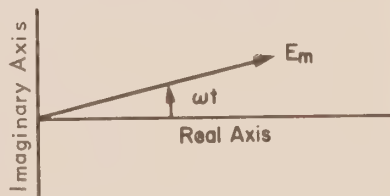


FIG. 3-1 Phasor Diagram

The projection of the phasor on the real axis varies sinusoidally if the phasor is rotated at a constant angular frequency. In fact, the projected value of the phasor is equal to $E_m \cos \omega t$, and one can convert the cosine term to a sine term by rotating the phasor through 90° or $\pi/2$ radians. Equation (3-2) results

$$\begin{aligned} E_m \sin \omega t &= \operatorname{Re} E_m \angle \omega t - \pi/2 \\ &= \operatorname{Re} E_m \left[\cos \left(\omega t - \frac{\pi}{2} \right) + j \sin \left(\omega t - \frac{\pi}{2} \right) \right] \end{aligned} \quad (3-2)$$

The symbol Re means that one takes only the real part which is the projected value of the phasor on the real axis.

A similar expression for $\cos \omega t$ can be derived, and Eq. (3-3) illustrates several ways of expressing $\cos \omega t$

$$\begin{aligned} e &= E_m \cos \omega t = E_m \left(\frac{e^{j\omega t} + e^{-j\omega t}}{2} \right) \\ &= \operatorname{Re} E_m \angle \omega t \text{ volts} \end{aligned} \quad (3-3)$$

The Taylor series for the sine and cosine are also of interest at times, and these are indicated by Eqs. (3-4) and (3-5), respectively, where θ is in radians

$$\sin \theta = \theta - \frac{\theta^3}{3!} + \frac{\theta^5}{5!} - \frac{\theta^7}{7!} + \dots \quad (3-4)$$

$$\cos \theta = 1 - \frac{\theta^2}{2!} + \frac{\theta^4}{4!} - \frac{\theta^6}{6!} + \dots \quad (3-5)$$

Complex Algebra and Phasor Diagrams are applicable to the analysis of ac circuits, and certain mathematical rules must be established before one proceeds.

The addition of vector quantities is defined as follows where j is equal to $\sqrt{-1}$:

$$(a + jb) + (c + jd) = (a + c) + j(b + d)$$

Similarly, subtraction is defined as follows:

$$(a + jb) - (c + jd) = (a - c) + j(b - d)$$

Multiplication is as follows with j^2 equal to -1 :

$$(a + jb)(c + jd) = (ac - bd) + j(ad + bc)$$

Division is accomplished by rationalizing the denominator:

$$\frac{a + jb}{c + jd} = \frac{(a + jb)(c - jd)}{(c + jd)(c - jd)} = \frac{(ac + bd) + j(bc - ad)}{c^2 + d^2}$$

In multiplication and division, the polar form is more convenient than the rectangular form, and the conversion from rectangular to polar is as follows:

$$a + jb = c \angle \beta$$

where

$$c = \sqrt{a^2 + b^2}$$

$$\beta = \tan^{-1}(b/a)$$

The conversion from polar form to rectangular is a similar application of trigonometry:

$$c \angle \beta = c(\cos \beta + j \sin \beta)$$

Multiplication of polar quantities is accomplished by using the following rule:

$$(A \angle \alpha)(B \angle \beta) = AB \angle \alpha + \beta$$

The rule for division is as follows:

$$\frac{A \angle \alpha}{B \angle \beta} = \frac{A \angle \alpha - \beta}{B}$$

When polar quantities are multiplied, the magnitudes are multiplied and the angles added algebraically. When polar quantities are divided, the magnitudes are divided and the angle in the denominator is subtracted algebraically from the angle in the numerator.

Example 3-1

A voltage of 115 vrms $\angle 0^\circ$ is applied across an impedance of $10 + j10 \Omega$. What is the current that flows through the impedance, and how many watts are dissipated?

$$I = \frac{E}{Z} = \frac{(115 + j0)(10 - j10)}{(10 + j10)(10 - j10)} = \frac{115(10 - j10)}{200}$$

$$I = 5.75 - j5.75 = 8.1 \angle -45^\circ \text{ amperes}$$

The magnitude of the current is 8.1 A rms, and the current lags the voltage by 45° . An alternate way of solving the problem is to convert the denominator to polar form

$$I = \frac{E}{Z} = \frac{115 \angle 0^\circ}{14.1 \angle 45^\circ} = 8.1 \angle -45^\circ \text{ amperes}$$

Real power is equal to the magnitude of the voltage times the component of current which is in phase with the voltage. One can use the formula for power which was derived in Chap. 2

$$P = EI \cos \theta = (115)(8.1) \cos (-45^\circ) = 6.6 \times 10^2 \text{ watts}$$

An alternate method is to use the rectangular form and take only the component of current which is in phase with the voltage

$$P = (115)(5.75) = 6.6 \times 10^2 \text{ watts}$$

3-2 COMPLEX POWER

The consideration of power is important, and the Circuit Designer must be adept in solving the various types of problems involving power. The phasor diagram of Fig. 3-2 is used to illustrate how one solves for power where both the voltage and the current are complex.

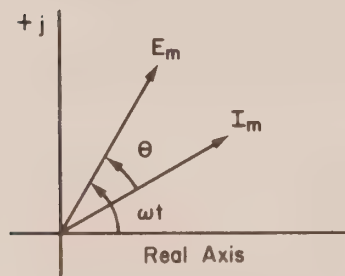


FIG. 3-2 Phasor Diagram — Power

Real power is *not* the product of the real voltage component and the real current component. It is instead the product of the magnitude of the voltage and the component of current which is in phase with the voltage. Also, one must be careful to recognize whether or not peak values rather than rms

values are used. Power in watts is equal to the rms voltage times the rms current times the cosine of the angle between the two. For the case depicted in Fig. 3-2, power is a familiar expression:

$$P = \left(\frac{E_m}{2} I_m \right) \cos \theta \text{ watts}$$

Although the phase angle θ is constant, the angle ωt varies with time, and the case depicted in Fig. 3-2 illustrates the

position of the phasors at a given instant in time. Both phasors are rotating counterclockwise at a constant angular frequency of ω radians per second. Average power, however, does not vary as a function of time.

The two phasors can be expressed in polar form with respect to the real axis as follows where E and I are rms quantities:

$$E = |E| \angle \omega t$$

$$I = |I| \angle \omega t - \theta$$

It is known that real power is equal to the magnitude of the rms voltage E times the magnitude of the rms current I times the cosine of the angle between the two. One might reason incorrectly that real power could be found by taking the product of the voltage phasor, the current phasor, and the cosine of the resultant angle. The result of such a computation is the following:

$$EI = |E| |I| \angle \omega t \angle \omega t - \theta = |E| |I| \angle 2\omega t - \theta$$

$$P \neq |E| |I| \cos(2\omega t - \theta)$$

However, it has already been established that real power is equal, in fact, to $|E| |I| \cos \theta$. If the angle of the current phasor were $\theta - \omega t$, the computation for real power would be correct. This angle is obtained by taking the conjugate of the current phasor. The conjugate of I is written as $\bar{I}$

$$I = |I| \angle \omega t - \theta$$

$$\bar{I} = |I| \angle -\omega t + \theta$$

It is now apparent that the product of the voltage phasor, the conjugate of the current phasor, and the cosine of the resultant angle is the real power in watts

$$P = \text{Real part of } (E\bar{I}) = EI \cos \theta \text{ watts}$$

Power in watts is merely the real part of the volt-amperes, and the real part is extracted by multiplying the volt-amperes by $\cos \theta$. Thus, the volt-ampere product is known.

$$VA = E\bar{I} = |EI| \angle \theta$$

Real power is defined by Eq. (3-6) where the symbol Re means that the real part of the product is to be taken

$$P = Re \, E\bar{I} \text{ watts} \quad (3-6)$$

If current and voltage are specified in rectangular form, one can find power by converting to polar form and using Eq. (3-6). However, power can be found directly, and Example 3-2 is used to illustrate the method.

Example 3-2

Find the average power being dissipated where the voltage and current are specified as follows:

$$E_m = 70.7 + j70.7 \text{ volts}$$

$$I_m = 8.66 + j5 \text{ amperes}$$

The angle of interest is the phase angle between current and voltage. The rectangular expressions imply an angle with respect to the real axis, and a conversion is required to obtain the true phase angle between current and voltage. In the polar case, the angles were simply subtracted. The same thing is accomplished in the rectangular case by multiplying the voltage term by the conjugate of the current term. The conjugate of $a + jb$ is defined as $a - jb$

$$P = (70.7 + j70.7)(8.66 - j5) = 966 + j259$$

The current and voltage were expressed in peak values, so this expression must be divided by a factor of 2 to yield average power:

$$P_{av} = \frac{966 + j259}{2} = 483 + j129.5 \text{ VA}$$

The answer is in volt-amperes, and the problem is to find the real power. One method would be to convert to the polar form and multiply the magnitude of P by the cosine of the resultant angle, but the answer is already apparent in the rectangular form as the real part of P or 483 watts.

Real power is defined by Eq. (3-6), whether the current and voltage are expressed in polar or rectangular form. The expression for power, $P = 483 + j129.5$, is plotted in Fig. 3-3. The magnitude of P is found by taking the square root of the sum of the squares or by using trigonometry. The answer is 500 VA.

The reactive power or vars is 129.5, and the real power is 483 watts.

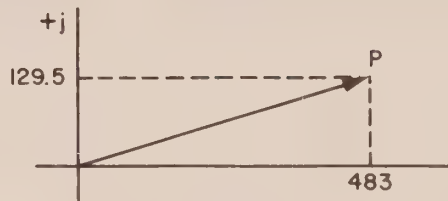


FIG. 3-3 Complex Power

In a circuit which is essentially inductive, the current lags the voltage and, conversely, the current leads the voltage in an essentially capacitive circuit. It is often desirable to tune a given load so that the reactive power (vars or kvars) is zero. The usual problem involves an inductive circuit with a lagging power factor, and capacitors are added to obtain unity power factor. In this case, it is the reactive power which must be determined. In fact, capacitors are often specified in vars or kvars for power factor correction. Example 3-3 is used to illustrate how a complex load impedance is tuned.

Example 3-3

From measurements on a parallel RL circuit it is known that $120\text{ V } \angle 0^\circ$ is applied across the circuit, and that the line current is $10 \angle -45^\circ$ A. The problem is to tune the load for unity power factor and to solve for the line current after tuning. The current is lagging the voltage, so capacitors must be added in parallel with the load. The answer can be found quite readily by solving for the reactive power.

$$\text{vars} = EI \sin \theta = (1200)(.707) = 848$$

The rating of the capacitor could be specified as 848 vars or 0.848 kvars.

Since a parallel circuit is specified, the tuned line current is equal to the real part of the original current or 7.07 A. However, it is instructive to draw a diagram such as that in Fig. 3-4.

Real power is defined by Eq. (3-6), and complex power is defined by the same equation before the real part is taken. In this case, power is the following:

$$P = (120 \angle 0^\circ)(10 \angle 45^\circ) = 1200 \angle 45^\circ \text{ VA}$$

$$W = 1200 \cos 45^\circ = 848$$

$$\text{vars} = 1200 \sin 45^\circ = 848$$

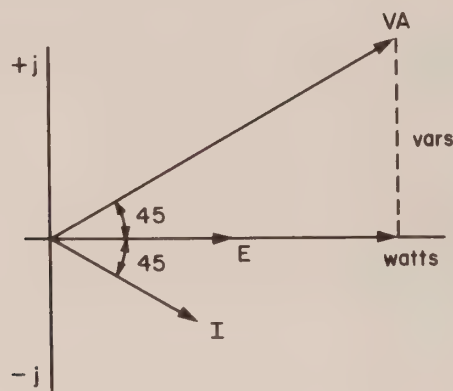


FIG. 3-4 Diagram for Example 3-3

The magnitude of the capacitive reactance can be calculated in several ways. The most direct way is as follows:

$$\begin{aligned}\frac{E^2}{X_C} &= 848 \text{ vars} \\ |X_C| &= \frac{(120)^2}{848} = 17 \Omega\end{aligned}$$

Another method of solving for X_C is to calculate the magnitude of the reactive current

$$I = 10 \angle -45 = 7.07 - j7.07 \text{ amperes}$$

If a current of $+j7.07$ A were added to the line current, it would then be totally real. The added current is obtained by connecting a capacitor in parallel with the load, and the capacitive reactance is readily calculated by Ohm's Law to be $-j17 \Omega$.

If the line frequency is assumed to be 60 cps, the required capacitance is:

$$\begin{aligned}X_C &= \frac{1}{\omega C} \\ C &= \frac{1}{(377)(17)} = 156 \mu\text{F}\end{aligned}$$

The voltage rating of the capacitor must be greater than the peak line voltage of $120\sqrt{2}$ volts.

3-3 RESISTOR-CAPACITOR CIRCUITS

Passive circuits are analyzed rather easily, and yet mistakes are frequently made. Such mistakes can be minimized by

establishing a given method for solving all typical problems associated with passive circuits. Although series and parallel circuits are analyzed in a similar way, one must remember that the defining equations are different. Consider the series circuit depicted in Fig. 3-5.

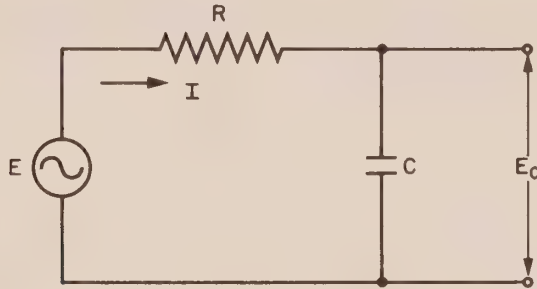


FIG. 3-5 Series RC Circuit

This simple circuit can be analyzed for a surprising number of quantities. For instance, how many volt-amperes are being delivered by the voltage generator, how many watts are being dissipated, what is the impedance of the circuit, what is the line current, what is the magnitude of the voltage across the capacitor, what is the phase of E_C with respect to E , and what is the voltage across the resistor?

Obviously, one would solve for only the desired quantity in a practical situation, but one must be capable of solving for any particular. A complete solution is best started by solving for the series impedance as defined by Eq. (3-7).

$$Z = R - jX_C \text{ ohms} \quad (3-7)$$

Equation (3-7) can be plotted as an impedance triangle, and this is illustrated in Fig. 3-6. The circuit impedance can be expressed in polar form as a magnitude at an angle θ with respect to the real axis. The desired expression is defined by Eq. (3-8).

$$Z = |Z| \angle \theta \text{ ohms} \quad (3-8)$$

where

$$|Z| = \sqrt{(R)^2 + (-X_C)^2}$$

$$\theta = \tan^{-1} \left(\frac{-X_C}{R} \right)$$

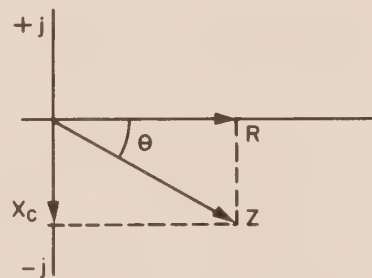


FIG. 3-6 Impedance Triangle

The line current by Ohm's Law is equal to the voltage E divided by the impedance Z as defined by either Eq. (3-7) or Eq. (3-8)

$$I = \frac{E}{Z} = \frac{E}{R - jX_C} = \frac{E}{|Z| \angle \theta}$$

The voltage drop across the resistor is equal to the current I multiplied by the resistance R

$$E_R = IR = \frac{ER}{R - jX_C}$$

Likewise, the voltage across the capacitor is equal to $-jIX_C$, and the phase angle associated with the solution is the phase angle of E_C with respect to E

$$E_C = -jIX_C = \frac{-jEX_C}{R - jX_C}$$

A different mathematical form can be obtained by rationalizing the denominator:

$$E_C = \frac{-jEX_C}{R - jX_C} \frac{R + jX_C}{R + jX_C} = \frac{EX_C}{\sqrt{R^2 + X_C^2}} \angle \tan^{-1}(-R/X_C)$$

The phase angle of the voltage E_C is then equal to $\tan^{-1}(-R/X_C)$.

The volt-ampere calculation is simply the voltage E multiplied by the conjugate of the current I .

$$VA = \frac{E^2}{R + jX_C}$$

Real power is equal to the real part of the volt-amperes.

$$P = Re E\bar{I} = \frac{E^2}{|Z|} \cos \theta \text{ watts}$$

Example 3-4

Answers in numerical form are often easier to understand than answers in general form. Let the parameters in Fig. 3-5 be the following:

$$E = 100 \angle 0^\circ \text{ volts}$$

$$R = 3 \quad \Omega$$

$$X_C = -j4 = 4 \angle -90^\circ \text{ ohms}$$

The magnitude and phase of the impedance is calculated from Eq. (3-8)

$$|Z| = \sqrt{3^2 + 4^2} = 5 \quad \Omega$$

$$\theta = \tan^{-1} \left(\frac{-X_C}{R} \right) = \tan^{-1} \left(\frac{-4}{3} \right) = -53.1^\circ$$

$$Z = 5 \angle -53.1^\circ \quad \text{ohms}$$

The line current is calculated from Ohm's Law

$$I = \frac{E}{Z} = \frac{100 \angle 0^\circ}{5 \angle -53.1^\circ} = 20 \angle 53.1^\circ \text{ amperes}$$

The voltage across the resistor is equal to the current I multiplied by the resistance R

$$E_R = 60 \angle 53.1^\circ \text{ volts}$$

Similarly, the voltage across the capacitor is equal to the line current times the capacitive reactance:

$$E_C = [20 \angle 53.1^\circ] [4 \angle -90^\circ] = 80 \angle -36.9^\circ \text{ volts}$$

Volt-amperes are equal to the voltage E multiplied by the conjugate of the current:

$$VA = (100)(20) \angle -53.1^\circ = 2000 \angle -53.1^\circ$$

Power in watts is equal to the real part of the volt-amperes

$$P = 2,000 \cos(-53.1^\circ) = 1,200 \text{ watts}$$

Also, power is equal to the square of the magnitude of I multiplied by R

$$P = 3(20)^2 = 1,200 \text{ watts}$$

Parallel RC Circuits

Parallel circuits can be analyzed as easily as series circuits, but the equations are different and should not be confused

with the series case. Consider the parallel circuit of Fig. 3-7. The impedance of the circuit is *not* equal to $R - jX_C$. The parallel impedance is calculated as follows:

$$Z = \frac{(R)(-jX_C)}{R - jX_C} = \frac{-jRX_C}{R - jX_C} \frac{R + jX_C}{R + jX_C} = \frac{RX_C^2 - jR^2X_C}{R^2 + X_C^2}$$

$$Z = \frac{RX_C(X_C - jR)}{R^2 + X_C^2} = \frac{RX_C \left[\sqrt{R^2 + X_C^2} / \tan^{-1}(-R/X_C) \right]}{R^2 + X_C^2}$$

$$Z = \frac{RX_C / \tan^{-1}(-R/X_C)}{\sqrt{R^2 + X_C^2}} \text{ ohms} \quad (3-9)$$

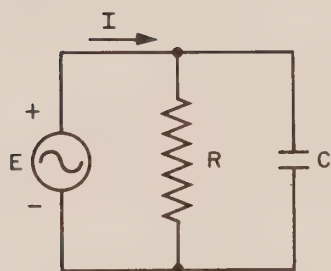


FIG. 3-7 Parallel RC Circuit

The line current can be calculated by dividing the voltage E by the impedance Z , but it is more easily found by solving independently for the current through the resistor and the current through the capacitor. The vector sum of these currents is then the line current

$$I_R = \frac{E}{R}$$

$$I_C = \frac{E}{-jX_C} = \frac{jE}{X_C}$$

$$I = E \left[\frac{1}{R} + \frac{j}{X_C} \right]$$

Since the line current can be calculated so readily in a given problem, it is often easier to solve for Z after solving for I , and another form for Z is expressed by Eq. (3-11)

$$Z = \frac{E}{I} = \frac{1}{1/R + j/X_C} \text{ ohms} \quad (3-11)$$

Volt-amperes are equal to the voltage E multiplied by the

conjugate of the current I

$$VA = E^2 \left[\frac{1}{R} - \frac{j}{X_C} \right]$$

Real power is all dissipated in the resistor

$$P = \frac{E^2}{R} \text{ watts}$$

The voltage across the resistor and the voltage across the capacitor are both equal to the generator voltage E . However, the current through the capacitor leads the voltage by 90° , and the current through the resistor is in phase with the voltage.

Example 3-5

The parameters in Fig. 3-7 are chosen to be the same as the series circuit in Example 3-4 to illustrate the differences in the answers

$$E = 100 \angle 0^\circ \text{ volts}$$

$$R = 3 \Omega$$

$$X_C = -j4 = 4 \angle -90^\circ \text{ ohms}$$

The line current is calculated by solving for I_R and I_C

$$I_R = \frac{100 \angle 0^\circ}{3} = 33.3 \angle 0^\circ \text{ amperes}$$

$$I_C = \frac{100 \angle 0^\circ}{4 \angle -90^\circ} = 25 \angle 90^\circ \text{ amperes}$$

$$I = 33.3 + j25 = 41.5 \angle 36.9^\circ \text{ amperes}$$

The impedance is equal to E divided by I

$$Z = \frac{E}{I} = \frac{100}{41.5 \angle 36.9^\circ} = 2.4 \angle -36.9^\circ \text{ ohms}$$

Volt-amperes are equal to $E\bar{I}$

$$VA = (100)(41.5) \angle -36.9^\circ = 4150 \angle -36.9^\circ$$

Power is equal to the real part of the volt-amperes or E^2/R

$$P = \frac{E^2}{R} = \frac{10^4}{3} = 3333 \text{ watts}$$

3-4 RESISTOR-INDUCTOR CIRCUITS

The mathematical expressions for RL circuits are very similar to RC circuits, and the methods of analysis are the same. A major difference is that current lags the voltage in inductive circuits and leads the voltage in capacitive circuits. A series RL circuit is depicted in Fig. 3-8.

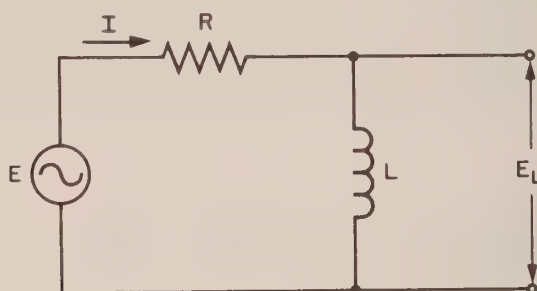


FIG. 3-8 Series RL Circuit

The line current, circuit impedance, power dissipated, etc. are found as before. The series impedance is defined by Eq. (3-12)

$$Z = R + jX_L \text{ ohms} \quad (3-12)$$

In polar form, the impedance is defined by Eq. (3-13):

$$Z = |Z| \angle \theta \text{ ohms} \quad (3-13)$$

where

$$|Z| = \sqrt{R^2 + X_L^2}$$

$$\theta = \tan^{-1} \left(\frac{X_L}{R} \right)$$

The line current is equal to the voltage E divided by the impedance Z

$$I = \frac{E}{R + jX_L} = \frac{E}{|Z| \angle \theta}$$

The voltage across the inductor is equal to jIX_L

$$E_L = \frac{(jX_L)(E)}{|Z|/\theta} = \frac{X_L E \angle 90^\circ - \theta}{|Z|}$$

The phase angle of E_L is equal to $(90 - \theta)$ deg, but it may be found more readily from a different expression

$$\text{Phase angle of } E_L = \tan^{-1} \left(\frac{R}{X_L} \right)$$

The volt-ampere calculation is simply the voltage E multiplied by the conjugate of the current I

$$VA = \frac{E^2}{R - jX_L}$$

Real power is equal to the real part of the volt-amperes

$$P = \text{Re } E\bar{I} = \frac{E^2 \cos \theta}{|Z|} \text{ watts}$$

Example 3-6 is used to illustrate how one calculates the various quantities associated with series RL circuits.

Example 3-6

The parameters in the circuit of Fig. 3-8 are defined as follows:

$$E = 100 \angle 0^\circ \text{ volts}$$

$$R = 3 \ \Omega$$

$$X_L = j4 = 4 \angle 90^\circ$$

The magnitude and phase of the circuit impedance is calculated from Eq. (3-13)

$$Z = \sqrt{3^2 + 4^2} \angle \tan^{-1}(4/3) = 5 \angle 53.1^\circ$$

The line current is calculated from Ohm's Law

$$I = \frac{E}{Z} = \frac{100 \angle 0^\circ}{5 \angle 53.1^\circ} = 20 \angle -53.1^\circ \text{ amperes}$$

The voltage across the resistor is equal to IR

$$E_R = 60 \angle -53.1^\circ \text{ volts}$$

Similarly, the voltage across the inductor is equal to the line current times the inductive reactance

$$E_L = (20 \angle -53.1^\circ) (4 \angle 90^\circ) = 80 \angle 36.9^\circ \text{ volts}$$

Volt-amperes are equal to $E\bar{I}$

$$VA = (100) (20) \angle 53.1^\circ = 2,000 \angle 53.1^\circ$$

Power in watts is equal to the real part of the volt-amperes

$$P = 2,000 \cos (53.1^\circ) = 1,200 \text{ W}$$

Also, power is equal to the square of the magnitude of I multiplied by R

$$P = 3(20)^2 = 1,200 \text{ W}$$

The results of this example are identical to those of the RC circuit in Example 3-4 except for the polarity of certain phase angles.

Parallel RL Circuits

Parallel RL circuits are analyzed in the same way as parallel RC circuits. A parallel circuit is depicted in Fig. 3-9

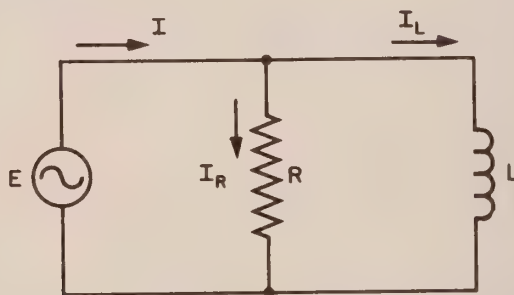


FIG. 3-9 Parallel RL Circuit

The impedance of the circuit is *not* equal to $R + jX_L$. The impedance is defined by Eq. (3-14)

$$Z = \frac{1}{1/R - j/X_L} \text{ ohms} \quad (3-14)$$

The line current is given by Eq. (3-15)

$$I = E \left(\frac{1}{R} - \frac{j}{X_L} \right) \text{ amperes} \quad (3-15)$$

Example 3-7 illustrates how a parallel RL circuit is analyzed.

Example 3-7

The parameters of the circuit in Fig. 3-9 are defined as follows:

$$E = 100 \angle 0^\circ \text{ volts}$$

$$R = 3 \, \Omega$$

$$X_L = j4 = 4 \angle 90^\circ$$

The line current is calculated by solving for I_R and I_L

$$I_R = \frac{100 \angle 0^\circ}{3} = 33.3 \angle 0^\circ \text{ amperes}$$

$$I_L = \frac{100 \angle 0^\circ}{4 \angle 90^\circ} = 25 \angle -90^\circ \text{ amperes}$$

$$I = 33.3 - j25 = 41.5 \angle -36.9^\circ \text{ amperes}$$

The impedance is equal to E divided by I

$$Z = \frac{E}{I} = \frac{100 \angle 0^\circ}{41.5 \angle -36.9^\circ} = 2.4 \angle 36.9^\circ$$

Volt-amperes are equal to $E\bar{I}$

$$VA = (100)(41.5) \angle 36.9^\circ = 4,150 \angle 36.9^\circ$$

Power is equal to the real part of the volt-amperes

$$P = 4,150 \cos(36.9^\circ) = 3333 \text{ W}$$

Power is also equal to E^2/R

$$P = \frac{100^2}{3} = 3333 \text{ W}$$

3-5 RCL CIRCUITS

A logical extension of the two previous paragraphs involves, of course, combination of all three elements in one circuit. The Circuit Designer has mastered an important portion of his field when he is able to solve rapidly and easily problems associated with series-parallel combinations of resistors, capacitors, and inductors.

Consideration of RCL circuits begins with the series circuit which is depicted in Fig. 3-10

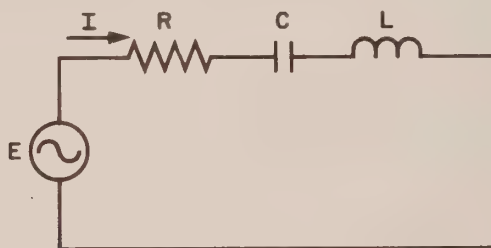


FIG. 3-10 Series RCL Circuit

The impedance of the circuit is defined by Eq. (3-16)

$$Z = R + j(X_L - X_C) \text{ ohms} \quad (3-16)$$

The magnitude of the impedance is defined by Eq. (3-17)

$$|Z| = \sqrt{R^2 + (X_L - X_C)^2} \text{ ohms} \quad (3-17)$$

The magnitude of the impedance Z is defined by Eq. (3-17) for a series circuit, and the equation is *not* true for a parallel circuit. Also, Eq. (3-16) is *not* valid for a parallel circuit.

The current I can be in phase with the voltage, lead the voltage, or lag the voltage depending upon whether X_C is equal to X_L , X_C is greater than X_L , or X_C is less than X_L . The current I is in phase with the voltage at the resonant frequency where X_C is equal to X_L . The impedance Z is, of course, a function of frequency.

Example 3-8 is used to illustrate how one calculates the various quantities associated with series RCL circuits.

Example 3-8

The parameters in Fig. 3-10 are specified as follows:

$$E = 100 \angle 0^\circ \text{ volts}$$

$$R = 3 \Omega$$

$$X_L = j4 = 4 \angle 90^\circ \Omega$$

$$X_C = -j5 = 5 \angle -90^\circ \Omega$$

The impedance is calculated from Eqs. (3-16) and (3-17)

$$Z = 3 + j(4 - 5) = 3 - j$$

$$|Z| = \sqrt{3^2 + (-1)^2} = 3.16 \Omega$$

In polar form, the impedance is as follows:

$$Z = 3.16 \angle \tan^{-1}(-1/3) = 3.16 \angle -18.4^\circ$$

The line current is equal to the voltage divided by the impedance

$$I = \frac{E}{Z} = \frac{100 \angle 0^\circ}{3.16 \angle -18.4^\circ} = 31.6 \angle 18.4^\circ$$

The volt-amperes are equal to $E\bar{I}$

$$VA = 3160 \angle -18.4^\circ$$

Power is equal to the square of the magnitude of I multiplied by R

$$P = (31.6)^2(3) = 3,000 \text{ W}$$

In this particular example, current leads the voltage (by 18.4°) because X_C is greater than X_L . The above results are valid for a given, fixed frequency where X_L is $j4 \Omega$ and X_C is $-j5 \Omega$.

Parallel RCL Circuits

Parallel RCL circuits can be solved quite readily provided one uses the proper method. It is important to remember that the impedance equations for series circuits do not apply to parallel circuits. The impedance of a parallel RCL circuit is not equal to $R + j(X_L - X_C)$, and the magnitude of the impedance is not equal to $\sqrt{R^2 + (X_L - X_C)^2}$. Consider the parallel circuit

of Fig. 3-11.

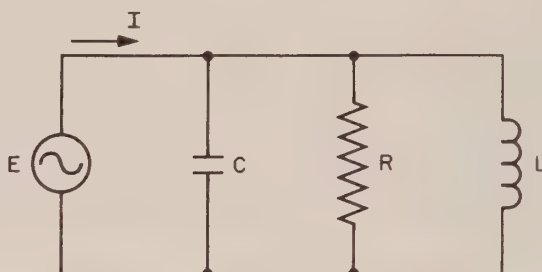


FIG. 3-11 Parallel *RCL* Circuit

The impedance of the parallel circuit can be found by taking the reciprocal of the sum of the reciprocals of the individual resistances and reactances

$$Z = \frac{1}{1/R + 1/jX_L - 1/jX_C}$$

$$Z = \frac{1}{1/R + j(X_C - X_L)} \text{ ohms} \quad (3-18)$$

In a practical problem, parallel impedance is often found by solving for the current I . The impedance Z is then equal to the voltage E divided by the current I . The current I is simply the vector sum of the branch currents

$$I = \frac{E}{R} + \frac{E}{jX_L} - \frac{E}{jX_C} \text{ amperes}$$

Volt-amperes are equal to $E\bar{I}$, and the power dissipated in watts is equal to the real part of $E\bar{I}$. Power is also equal to the square of the voltage E divided by the resistance R .

Example 3-9 is used to illustrate how one calculates the various quantities associated with parallel RCL circuits.

Example 3-9

The parameters in the circuit of Fig. 3-11 are defined as follows:

$$E = 100 \angle 0^\circ \text{ volts}$$

$$R = 3 \, \Omega$$

$$X_L = j4 = 4 \angle 90^\circ$$

$$X_C = -j5 = 5 \angle -90^\circ$$

The line current is found by solving for the individual currents

$$I_R = \frac{100}{3} = 33.3$$

$$I_L = \frac{100 \angle 0^\circ}{4 \angle 90^\circ} = 25 \angle -90^\circ = -j25$$

$$I_C = \frac{100 \angle 0^\circ}{5 \angle -90^\circ} = 20 \angle 90^\circ = j20$$

$$I = 33.3 + j(20 - 25) = 33.3 - j5 = 33.8 \angle -8.6^\circ$$

Impedance is found by dividing the voltage E by the current I

$$Z = \frac{100 \angle 0^\circ}{33.8 \angle -8.6^\circ} = 2.96 \angle 8.6^\circ \Omega$$

The volt-amperes are equal to $E\bar{I}$

$$VA = (100)(33.8) \angle 8.6^\circ = 3,380 \angle 8.6^\circ$$

Power is equal to E^2 divided by R

$$P = \frac{100^2}{3} = 3,333 \text{ W}$$

Series-parallel circuits are analyzed by applying the previously developed methods. More terms are involved as the circuits become more complex. Example 3-10 is used to illustrate how a typical problem is solved.

Example 3-10

The impedance of the series-parallel circuit which is depicted in Fig. 3-12 is to be found.

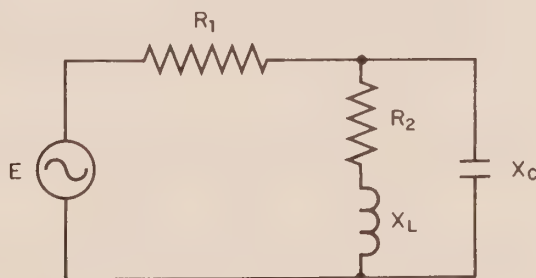


FIG. 3-12 Series-Parallel Circuit

The parameters are given as follows:

$$E = 100 \text{ V}$$

$$R_1 = 100 \text{ } \Omega$$

$$R_2 = 200 \text{ } \Omega$$

$$X_L = j2,000 \text{ } \Omega$$

$$X_C = -j3,000 \text{ } \Omega$$

The impedance is equal to R_1 plus the series-parallel impedance of the other three parameters

$$Z = R_1 + \frac{(R_2 + jX_L)(-jX_C)}{R_2 + jX_L - jX_C}$$

$$Z = R_1 + \frac{X_L X_C - jR_2 X_C}{R_2 + j(X_L - X_C)}$$

$$Z = 100 + \frac{6 \times 10^6 - j6 \times 10^5}{200 + j(-1000)}$$

$$= 100 + \frac{6.03 \times 10^6 \angle -5.7^\circ}{1.02 \times 10^3 \angle -78.7^\circ}$$

$$= 100 + 5.9 \times 10^3 \angle 73^\circ$$

$$= 100 + 1.73 \times 10^3 + j5.65 \times 10^3$$

$$= 1.83 \times 10^3 + j5.65 \times 10^3$$

$$Z = 6 \times 10^3 \angle 72.1^\circ \text{ } \Omega$$

3-6 TRANSFORMATIONS-DELTA TO WYE

There are certain circuit configurations which can best be simplified by a transformation of Δ to Y or vice versa. Delta and wye circuits are depicted in Fig. 3-13.

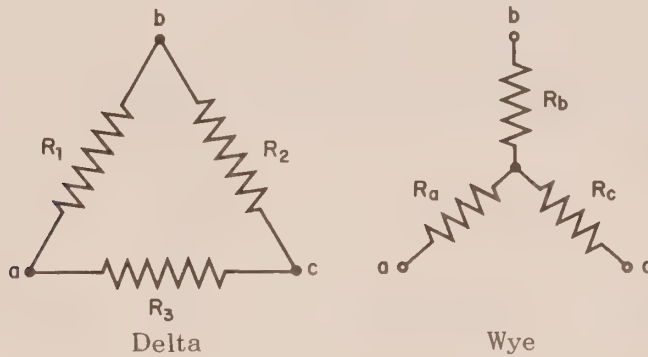


FIG. 3-13 Delta-Wye Transformation

For the transformation to be valid, the resistance between any two of the terminals *abc* must be the same for either circuit. The desired equations can be derived quite readily and are merely listed below.

Delta to Wye Conversion Equations

$$R_a = \frac{R_1 R_3}{R_1 + R_2 + R_3} \text{ ohms} \quad (3-19)$$

$$R_b = \frac{R_1 R_2}{R_1 + R_2 + R_3} \text{ ohms} \quad (3-20)$$

$$R_c = \frac{R_2 R_3}{R_1 + R_2 + R_3} \text{ ohms} \quad (3-21)$$

Wye to Delta Conversion Equations

$$R_1 = \frac{R_a R_b + R_b R_c + R_c R_a}{R_c} \text{ ohms} \quad (3-22)$$

$$R_2 = \frac{R_a R_b + R_b R_c + R_c R_a}{R_a} \text{ ohms} \quad (3-23)$$

$$R_3 = \frac{R_a R_b + R_b R_c + R_c R_a}{R_b} \text{ ohms} \quad (3-24)$$

The delta-wye transformation is applied to a bridge circuit in Example 3-11.

Example 3-11

The assignment is to solve for all the branch currents in the circuit which is depicted in Fig. 3-14

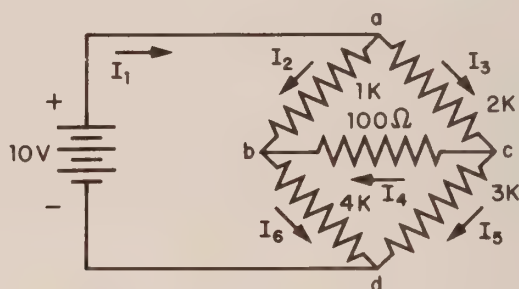
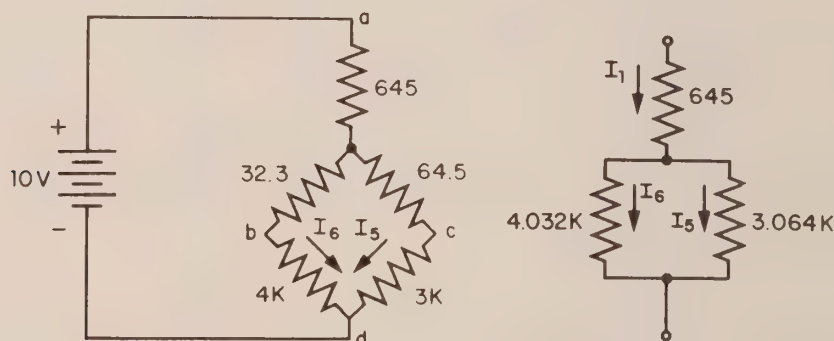


FIG. 3-14 Bridge Problem

The circuit is converted to a different form by applying the $\Delta - Y$ transformation.

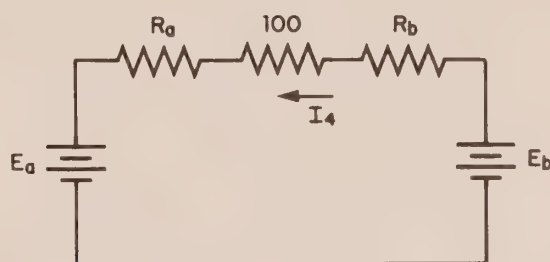


$$I_1 = \frac{10}{1750 + 645} = 4.18 \text{ mA}$$

$$I_5 = \frac{4.18}{1 + (3.06/4.03)} = 2.38 \text{ mA}$$

$$I_6 = 4.18 - 2.38 = 1.80 \text{ mA}$$

One could solve for the currents I_2 , I_3 , and I_4 by applying the $\Delta - Y$ transformation to the second delta circuit in Fig. 3-14, but the current I_4 can be found quite easily by using Thévenin's Theorem twice on the original circuit. The application of Thévenin's Theorem yields the following circuit:



$$E_a = \frac{(4)(10)}{5} = 8 \text{ V}$$

$$E_b = \frac{(3)(10)}{5} = 6 \text{ V}$$

$$R_a = \frac{(1)(4)}{5} = 800 \text{ } \Omega$$

$$R_b = \frac{(2)(3)}{5} = 1,200 \text{ } \Omega$$

$$I_4 = \frac{6 - 8}{1,200 + 800 + 100}$$

$$I_4 = -.95 \text{ mA}$$

The currents I_2 and I_3 are found as follows:

$$I_3 = I_5 + I_4 = 2.38 - 0.95 = 1.43 \text{ mA}$$

$$I_2 = I_1 - I_3 = 4.18 - 1.43 = 2.75 \text{ mA}$$

Thus, the complete solution to the problem is:

$$I_1 = 4.18 \text{ mA}$$

$$I_2 = 2.75 \text{ mA}$$

$$I_3 = 1.43 \text{ mA}$$

$$I_4 = -.95 \text{ mA}$$

$$I_5 = 2.38 \text{ mA}$$

$$I_6 = 1.80 \text{ mA}$$

3-7 BRIDGE CIRCUITS

Unknown values of resistors, capacitors, and inductors can be determined by making use of an impedance bridge. The unknown component is connected across one arm of the bridge, and a second arm is varied in calibrated steps until bridge balance is obtained. The unknown value is then read from the bridge dials.

Although such an instrument can be operated successfully without a knowledge of bridge circuits, it is instructive to explore the mathematics associated with bridge circuits. A resistance bridge is depicted in Fig. 3-15

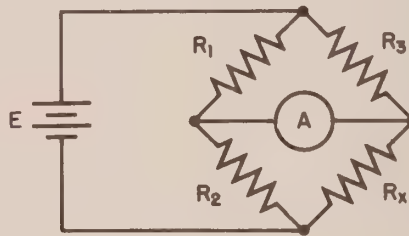


FIG. 3-15 Resistance Bridge

When the bridge is at balance, no current conducts through the ammeter, and, therefore, the voltage drop across resistor R_2 is the same as the voltage drop across the unknown resistor R_X . One can solve for the unknown resistor in terms of the other three resistors as follows:

$$\frac{ER_2}{R_1 + R_2} = \frac{ER_X}{R_3 + R_X}$$

$$R_2(R_3 + R_X) = R_X(R_1 + R_2)$$

$$R_2R_3 + R_2R_X = R_1R_X + R_2R_X$$

$$R_X = \frac{R_2R_3}{R_1} \text{ ohms} \quad (3-25)$$

The method of analysis is the same when reactive components are involved although the answer is somewhat more difficult to derive. Consider the bridge circuit which is depicted in Fig. 3-16

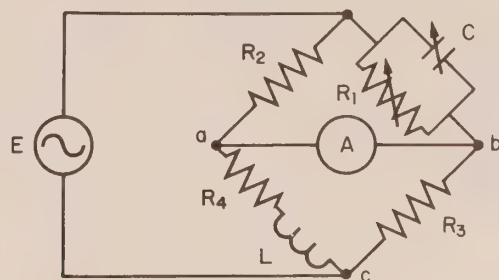


FIG. 3-16 Bridge Circuit

The problem is to derive the relationship at balance that exists between the unknown resistance R_4 , the unknown inductance L , and the other parameters of the bridge. At balance, the voltage from point a to point c is equal to the voltage from point b to point c . Let the parallel impedance of R_1 and X_C be Z_1 , and let the series impedance of R_4 and X_L be Z_2

$$\frac{R_3}{R_3 + Z_1} = \frac{Z_2}{R_2 + Z_2}$$

$$Z_2 = \frac{R_3 R_2 + R_3 Z_2}{R_3 + Z_1} = \frac{R_3 R_2}{R_3 + Z_1} + \frac{R_3 Z_2}{R_3 + Z_1}$$

$$Z_2 \left(1 - \frac{R_3}{R_3 + Z_1} \right) = \frac{R_3 R_2}{R_3 + Z_1}$$

$$Z_2 = \left(\frac{R_3 R_2}{R_3 + Z_1} \right) \left(\frac{R_3 + Z_1}{Z_1} \right) = \frac{R_2 R_3}{Z_1}$$

$$Z_2 = R_4 + jX_L = \frac{R_2 R_3}{Z_1}$$

$$Z_1 = \frac{-(R_1)(jX_C)}{R_1 - jX_C}$$

$$Z_2 = \frac{R_2 R_3}{Z_1} = \left(R_2 R_3 \right) \left(\frac{R_1 - jX_C}{-(R_1)(jX_C)} \right)$$

$$Z_2 = R_4 + jX_L = \frac{R_2 R_3}{R_1} - \frac{R_2 R_3}{jX_C}$$

At balance, the real terms must be equal, and the imaginary terms must be equal

$$R_4 = \frac{R_2 R_3}{R_1} \text{ ohms} \quad (3-26)$$

$$jX_L = \frac{R_2 R_3}{-jX_C}$$

$$X_L = \frac{R_2 R_3}{X_C}$$

$$\omega L = \omega R_2 R_3 C$$

$$L = R_2 R_3 C \text{ henries} \quad (3-27)$$

Equations (3-26) and (3-27) are valid for the particular bridge circuit depicted in Fig. 3-16, and should not be applied to bridge circuits at random. If the unknown quantities are R_1 and C , they can also be determined from Eqs. (3-26) and (3-27).

The engineering student is frequently asked to solve an unbalanced bridge problem. The parameter of interest is usually the current through the null detector. Several methods are available to solve such a problem, but the application of Thévenin's Theorem is perhaps the easiest. Example 3-12 is used to illustrate the method.

Example 3-12

The problem is to find the current I in the circuit which is depicted in Fig. 3-17

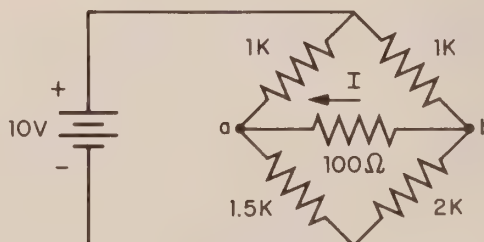
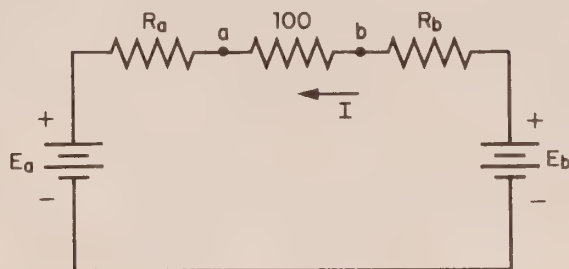


FIG. 3-17 Bridge Example

Application of Thévenin's Theorem to each half of the circuit yields the following equivalent circuit:



$$E_a = \frac{(1.5)(10)}{1 + 1.5} = 6 \text{ V}$$

$$E_b = \frac{(2)(10)}{2 + 1} = 6.667 \text{ V}$$

$$R_a = \frac{(1.5)(1)}{1 + 1.5} = 600 \text{ } \Omega$$

$$R_b = \frac{(2)(1)}{3} = 667 \text{ } \Omega$$

$$I = \frac{E_b - E_a}{R_a + R_b + 100} = \frac{0.667}{1,367}$$

$$I = 0.486 \text{ mA}$$

3-8 DESIGN EXAMPLE

It is known that a certain power system is of the form shown in Fig. 3-18. Measurements indicate that the magnitude of the line current I is 10 A, the magnitude of the output voltage E_o is equal to 20 V, and the phase of the voltage E_o with respect to the generator voltage E is $+30^\circ$ (lagging line current but the output voltage leads the input voltage). The assignment is to add a capacitor which will tune the system to unity power factor. The other parameters of the circuit are not known.

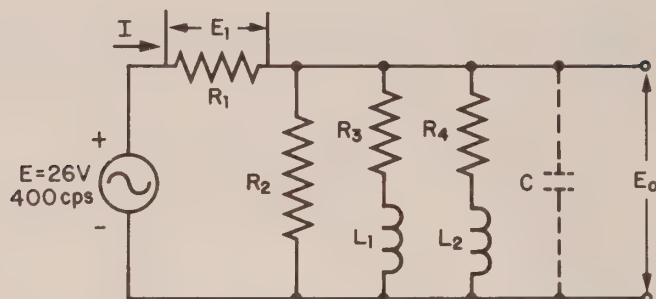


FIG. 3-18 Power-Factor Correction Problem

A phasor diagram of the specified voltages is drawn in Fig. 3-19

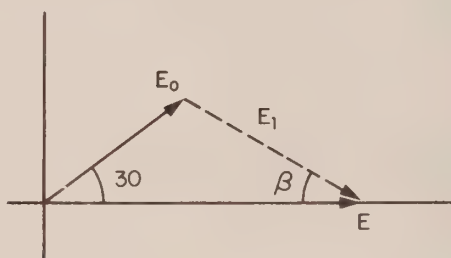


FIG. 3-19 Phasor Diagram for Design Example

It is known from Kirchhoff's Principles that the sum of the voltage drops around a closed circuit is equal to zero. That is, the vector sum of E_0 and E_1 must be equal to E . Therefore, the voltage drop across resistor R_1 can be drawn on the phasor diagram. The basic problem is to find the phase of the line current with respect to the input voltage. Since the line current is in phase with the voltage drop across resistor R_1 , the phase angle of the line current with respect to the input voltage is the same as the phase angle of the voltage E_1 . The methods of trigonometry are used to find the phase angle β

$$E_1 = \sqrt{E^2 + E_0^2 - 2EE_0 \cos 30^\circ}$$

$$= 13.24 \quad \text{V}$$

$$\sin \beta = \frac{E_0 \sin 30^\circ}{E_1}$$

$$= 0.752$$

$$\beta = 48.8^\circ$$

If the phasor E_1 is translated back to the origin, the angle of the phasor with respect to the real axis will be -48.8° . Thus, the phase angle of the line current with respect to the input voltage is equal to -48.8° which agrees with the premise that current should lag the voltage in an inductive circuit. The reactive power can now be calculated

$$\text{vars} = E\bar{I} \sin \theta = (26)(10)(\sin 48.8^\circ)$$

$$\text{vars} = 196$$

The magnitude of the capacitive reactance is found as follows:

$$X_C = \frac{E_o^2}{\text{vars}} = \frac{(20)^2}{196}$$

$$X_C = 2.04 \quad \Omega$$

The required value of capacitance is determined quite readily

$$C = \frac{1}{\omega X_C} = \frac{1}{(2,513)(2.04)} = 195 \mu F$$

$$C \cong 200 \mu F$$

After the circuit is tuned, certain parameters are of interest. What is the line current, what is the output voltage E_o , and how much power is delivered by the voltage generator? The original circuit is redrawn in a simplified form in Fig. 3-20, and depicts the untuned case.

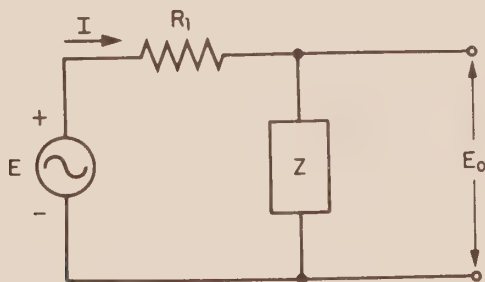


FIG. 3-20 Equivalent Circuit

Since the line current is now a known quantity, the impedance Z

can be calculated

$$Z = \frac{E_o}{I} = \frac{20 \angle 30^\circ}{10 \angle -48.8^\circ}$$

$$Z = 2 \angle 78.8^\circ \quad \Omega$$

The added capacitive reactance in parallel with the impedance Z must be equal to a new impedance which is completely real. If this requirement is not satisfied, the tuned line current will not be in phase with the input voltage. In fact, the required capacitive reactance can be calculated from this requirement after the impedance Z is known. Let the impedance Z be equal to $R + jX_L$. The parallel impedance, including the capacitive reactance, is calculated as follows:

$$Z_p = \frac{(R + jX_L)(-jX_C)}{R + jX_L - jX_C} = \frac{X_L X_C - jRX_C}{R + j(X_L - X_C)}$$

$$Z_p = \frac{X_L X_C - jRX_C}{R + j(X_L - X_C)} \cdot \frac{R - j(X_L - X_C)}{R - j(X_L - X_C)}$$

$$Z_p = \frac{RX_C^2 - j[R^2X_C + X_L X_C(X_L - X_C)]}{R^2 + (X_L - X_C)^2}$$

If the tuning requirement is satisfied, the reactive term must be equal to zero

$$R^2X_C + X_L X_C(X_L - X_C) = 0$$

$$R^2 + X_L(X_L - X_C) = 0$$

$$X_C = \frac{R^2 + X_L^2}{X_L} \text{ ohms} \quad (3-28)$$

The required tuning reactance to achieve unity power factor can be determined from Eq. (3-28) if the impedance Z is known. The capacitive reactance is calculated by this method to check the previous result

$$Z = 2 / \underline{78.8^\circ} = .3884 + j1.962$$

$$X_C = \frac{R^2 + X_L^2}{X_L} = \frac{(.3884)^2 + (1.962)^2}{1.962}$$

$$X_C = 2.04 \ \Omega$$

The tuned impedance is equal to the real part of the impedance Z_p

$$Z_p = \frac{RX_C^2}{R^2 + (X_L - X_C)^2}$$

$$Z_p = \frac{(.3884)(2.04)^2}{(.3884)^2 + (1.962 - 2.04)^2}$$

$$Z_p \cong 10.2 \ \Omega$$

Also, the resistance R_1 can be calculated after solving for the untuned voltage E_1

$$R_1 = \frac{E_1}{I} = \frac{13.2}{10}$$

$$R_1 = 1.32 \ \Omega$$

The total tuned impedance Z_T is the sum of the impedance Z_p and the resistance R_1

$$Z_T = R_1 + Z_p = 1.3 + 10.2$$

$$Z_T = 11.5 \ \Omega$$

The tuned line current is calculated from Ohm's Law

$$I = \frac{26}{11.5} \cong 2.25 \text{ A}$$

The tuned output voltage is equal to the generator voltage minus

the voltage drop across resistor R_1

$$E_o = 26 - (2.25)(1.32) = 23.0 \text{ V}$$

The power delivered by the voltage generator is equal to the input voltage multiplied by the tuned line current

$$P = EI = (26)(2.25)$$

$$P = 58.5 \text{ W}$$

The results of the problem are summarized:

	Input VA	Line Current	Output Voltage
Untuned	260	10 A	20 V
Tuned	58.5	2.25	23

PROBLEMS

- 3-1 The values of the components in the blackbox which is depicted in Fig. 1 are to be determined from certain tests. An open-circuit test indicates the following transfer characteristic:

$$\frac{E_o}{E_{in}} = 0.707 \angle -45^\circ$$

The short-circuit output current is 2 mA, and the input voltage is 26 vrms at a frequency of 400 cps. What are the values of the resistor and the capacitor:

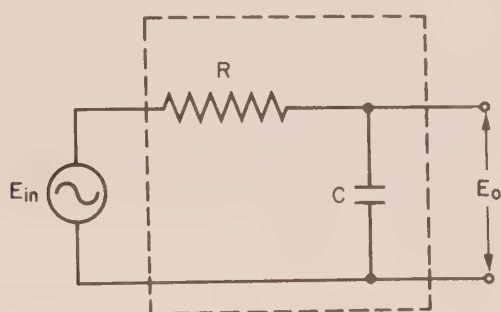


FIG. 1 Black Box Problem

- 3-2 How many watts are dissipated in the resistor which is depicted in Fig. 2? Assume that $X_L \gg R$. The voltage E is a full-wave-rectified sinusoidal signal with a peak voltage of 70 V.

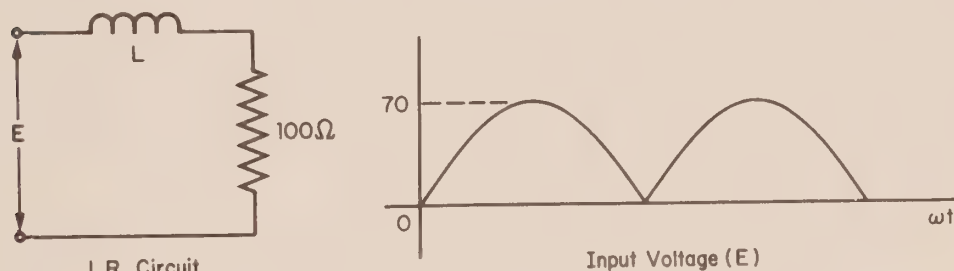


FIG. 2 Series LR Problem

- 3-3 What is the transfer characteristic, E_o/E_{in} , of the circuit depicted in Fig. 3?

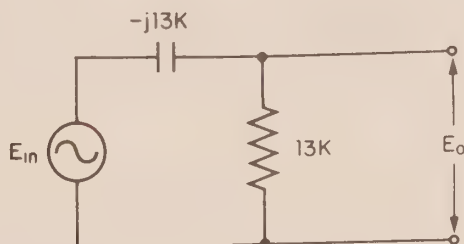


FIG. 3 Series RC Problem

- 3-4 In the circuit of Fig. 4, what is the phase angle of the line current with respect to the input voltage, and how many watts are dissipated in the circuit?

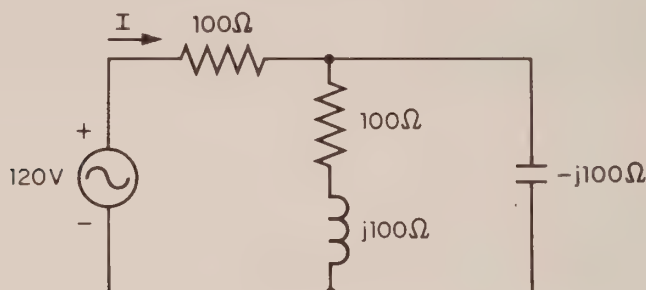


FIG. 4 Series-Parallel Problem

- 3-5 Two voltage generators of the same output amplitude and frequency are connected to a common load. See Fig. 5. Hint: The Principle of Superposition, or Norton's Theorem, is applicable to this problem.

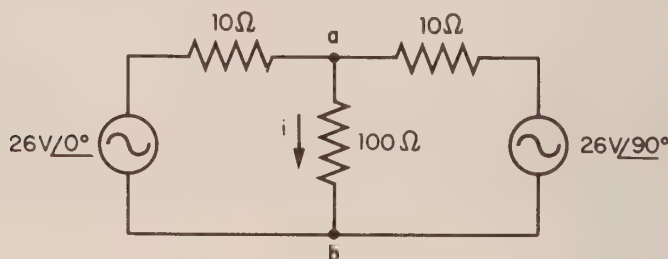


FIG. 5 Double Generator Problem

- What is the equation of the current i which flows through the 100-Ω resistor?
 - How many watts are dissipated in the 100-Ω resistor?
 - If an oscilloscope were connected from point a to point b in the circuit, would a single or double sinusoidal signal be observed?
- 3-6 The circuit of Fig. 6 is to be tuned to unity power factor by adding a capacitor from point a to point b . The following untuned parameters are measured:

$$E_{in} = 120 \angle 0^\circ \quad \text{V rms}$$

$$I = 1 \angle ? \quad \text{A rms}$$

$$E_o = 100 \angle 20^\circ \quad \text{V rms}$$

Calculate the capacitive reactance which must be added.

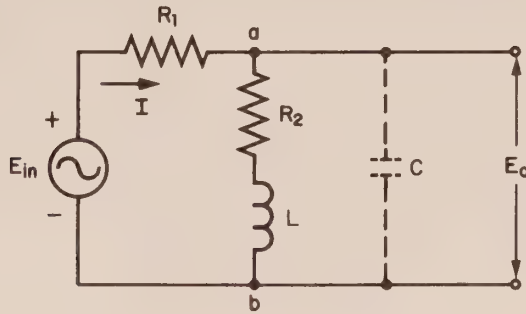


FIG. 6 Tuning Problem

- 3-7 A 60-cps sinusoidal signal with a peak amplitude of 170 V is full-wave-rectified. Design a filter of the type indicated by Fig. 7 which will reduce the 120-cps ripple voltage to less than 144-mV peak amplitude.

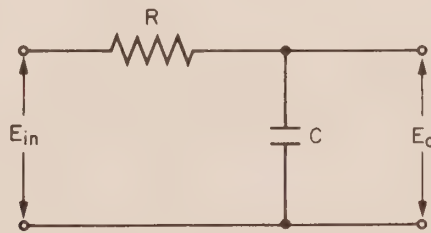


FIG. 7 Filter Problem

- 3-8 A 400-cps phase-shift oscillator is to be designed, and a network is required which will shift the phase of the input signal by 180° . The network is to be of the form indicated in Fig. 8. Specify the component values and the network transfer characteristic E_o/E_{in} (network attenuation).

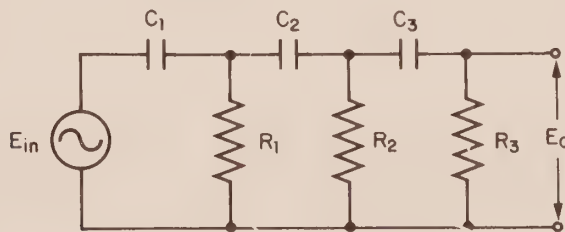


FIG. 8 Phase-Shift Problem

BIBLIOGRAPHY

- Fitzgerald, A. and D. Higginbotham: "Basic Electrical Engineering," chap. 3, McGraw-Hill Book Company, New York, 1957.
 Skilling, H.: "Electrical Engineering Circuits," chaps. 3 and 4, John Wiley & Sons, Inc., New York, 1957.

4

COMPONENTS

4-1 RESISTORS

The Circuit Designer must be familiar with the characteristics of many different components because the misapplication of a component can convert a good design into a poor one. Some components have been developed for certain specific applications and should not be used indiscriminately. The ordinary carbon-composition resistor, for instance, is usable in many circuits, but it is a poor choice for use in certain other circuits.

The standardization of parts has contributed, in general, to the advancement of modern technology, and this is true in the Electronics Industry, as well. Resistors have been standardized in terms of available values, tolerance, wattage rating, size, etc. Capacitors have likewise been standardized. It is desirable to use standard components wherever possible.

The purpose of this chapter is to introduce the reader to certain general characteristics of the various components which are readily available. The characteristics of specific components can be obtained from the manufacturer's specification sheets or from his sales office. A significant point is that the value of a particular component, such as a capacitor, will vary for a number of reasons. One must not assume, for instance, that the value of a capacitor is $100\ \mu\text{F}$ merely because $100\ \mu\text{F}$ is stamped on the case of the unit. The actual value may be nearly double the marked value, or considerably less than the marked value. One should always consult the manufacturer's specification sheet to determine the characteristics of a given component type. Only general considerations are covered in this chapter.

A color code has been established for use with fixed-composition resistors and some types of capacitors, and the code is indicated in Table 4-1.

Table 4-1 Color Code

Color	Number
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Gray	8
White	9

The color code is used to determine the nominal value of a given resistor. Each resistor has at least three colored bands around the body of the unit. Figure 4-1 illustrates the coding method.

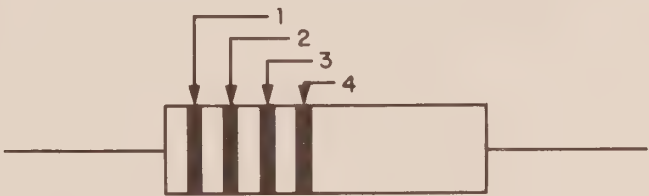


FIG. 4-1 Resistor Coding

The first and second bands indicate the two significant figures, and the third band indicates the number of zeros to be added after the first two numbers. The fourth band indicates the tolerance of the resistor where gold is ± 5 percent, silver is ± 10 percent, and no band is ± 20 percent. In other words, if the color of the first band were green, the second brown, the third red, and the fourth gold, the nominal value of the resistor would be $5,100\ \Omega$, ± 5 percent.

Nominal values are also standardized, and Table 4-2 indicates the standard significant figures for ± 5 -percent and

± 10-percent resistors. Standard wattage ratings for composition resistors include 1/4 W, 1/2 W, 1 W, and 2 W. These resistors can normally be procured if the desired value is within the range of 2.7 Ω to 22 MΩ. If the color of the third band is gold, it signifies that there should be a decimal point after the first significant figure. That is, the value of a 2.7-Ω resistor would be indicated by red, violet, and gold for bands one through three, respectively.

Table 4-2 Standard Resistor Values

± 5%	± 10%
10	10
11	
12	12
13	
15	15
16	
18	18
20	
22	22
24	
27	27
30	
33	33
36	
39	39
43	
47	47
51	
56	56
62	
68	68
75	
82	82
91	

The wattage rating of a resistor is determined by the maximum allowable internal temperature. In fact, the maximum power rating of components and semiconductors is generally determined by a temperature limitation. If a resistor fails

catastrophically in a circuit, the failure probably occurred because it simply became too hot. There may be a number of reasons why it overheated, but the failure is usually attributable to excessive heat. Thus, the basic problem is the removal of heat.

A 100- Ω , 2-W resistor is physically larger than a 100- Ω , 1-W resistor in order that a greater quantity of heat can be removed, in the steady state, from the unit. The primary heat transfer paths are from the resistor body to free air and from the leads to the rest of the circuitry. To illustrate the point, a 2-W resistor can be made to fail when it is dissipating only 1-W if it is insulated so that heat cannot escape. A resistor does not "care" what caused the excessive temperature; the result is the same, a unit failure. The excessive temperature may have been caused by high internal dissipation, high ambient temperature, proximity to other heat generating sources, etc. The Circuit Designer soon becomes aware of the facts that thermal considerations are important and that he must be concerned with how his circuit is packaged.

Since the absolute value of any resistor is temperature-dependent to some extent, it is desirable to operate resistors at a rating less than the maximum dissipation rating if stable resistance values are required by the circuit application. Resistors are often derated because of reliability considerations, as well. A "hot" resistor is less reliable than a "cold" resistor particularly if circuit reliability is a function of resistance stability. Many composition resistors can be operated at the published dissipation rating at ambient temperatures up to 70°C. They are then derated linearly to zero dissipation at about 130°C. However, it is common practice in military equipment to derate by 50 percent even at room temperature. That is, a resistor with a published rating of 1 W would be derated to 1/2 W at ambient temperatures up to 70°C. At temperatures above 70°C, the resistor would be derated linearly from 1/2 W to 0 at 130°C. Some composition resistors are usable at ambient temperatures of 150°C or higher, and the designer must consult the manufacturer's specification sheets for proper application of a given component.

An interesting point is that not every resistor can be operated at its indicated wattage rating. For instance, certain composition resistors with wattage ratings of 1/10 W are available with nominal resistance values up to 22 M Ω , but the manufacturer specifies a maximum continuous rated voltage of 150 V. Thus, resistors of values greater than 225 k Ω must be operated at less than 1/10 W. The maximum voltage limitation determines the power which can be dissipated in resistors with high values

of resistance. A 20-k Ω , 2-W resistor would require a working voltage of approximately 6.3 kV to dissipate 2 W. However, the maximum rated voltage may be 500 V, and the practical wattage rating would be much less than 2 W. A maximum voltage rating is imposed to limit the internal voltage gradient to a value which will not damage the resistor.

Every resistor has some voltage coefficient which may be negligible or appreciable as compared to some reference. That is, the value of a resistor is a function, to some extent, of the voltage across it. Figure 4-2 indicates the effect of voltage on resistance for three different types of resistors. One should use the manufacturer's specification sheets rather than Fig. 4-2 for design purposes, but it is apparent that the voltage coefficient of composition resistors is appreciable and considerably greater than the coefficient of wirewound or film resistors.

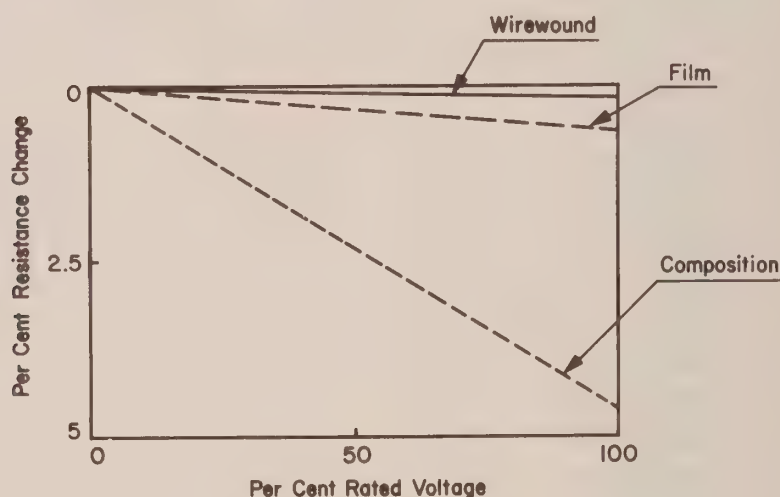


FIG. 4-2 Voltage Coefficient

Composition resistors are also affected by moisture. This may or may not be a problem depending upon the equipment-operating environment. The resistors will usually return to nominal values after a baking period at elevated temperature. Internally-generated heat is sometimes sufficient to restore equipment, after a period of time, to proper operation. For instance, television sets which are operated infrequently and which are located near the ocean may malfunction when first turned on after a prolonged off period. Proper operation can often be restored by simply leaving the set on for several hours. The components in military equipment are usually coated so that the effect of moisture is less than it is for comparable commercial equipment.

A composition resistor with current flowing through it acts as a noise generator. The noise voltage is a function of the

magnitude of the current and the magnitude of the resistor. A general number to establish the gross relationship is one microvolt of noise per volt across the resistor. The noise in microvolts per volt increases nonlinearly as the resistance increases. Composition resistors should not be used in the input stages of high-gain, low-noise amplifiers. Wirewound resistors are notably noise free, and other resistor types are also preferable to composition resistors for low-noise applications.

The temperature coefficient of resistance for composition resistors is nonlinear and a function of resistance value. This is indicated by the curves in Fig. 4-3 where the percent change in resistance is from the value at 25° C. Curve 1 is for a 10-K resistor, and curve 2 is for a 0.5-M Ω resistor.

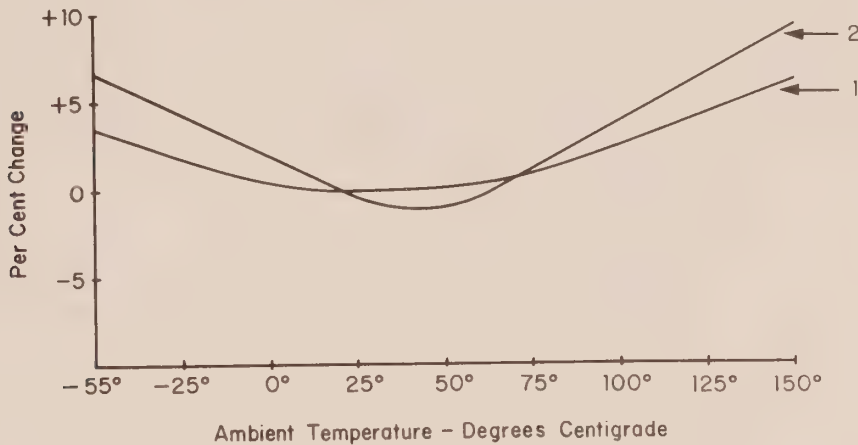


FIG. 4-3 Temperature Coefficient of Resistance

There is a random variation of appreciable proportions in the temperature coefficient for composition resistors. For instance, the manufacturer specifies that 10-K resistors can deviate from 25°C value by ± 3.5 percent at 85° C. Curve 1 in Fig. 4-3 indicates that a positive temperature coefficient can usually be expected at an ambient temperature of 85° C. A given resistor will usually repeat its particular temperature-coefficient curve, but variations from resistor to resistor can be expected even in resistors of the same value.

It is clear that the value of a composition resistor can vary for a number of reasons, and it is advantageous, when considering such resistors, to assign a general tolerance which will account for expected variations. One can mentally assume that ± 5 -percent resistors will vary from the nominal value, for all reasons, by ± 15 percent. Most resistors in a given family will not vary from the nominal value by as much as 15 percent, but circuits should be designed, wherever possible, to accommodate variations of this magnitude.

One might expect that the population density of a family of say ± 10 percent resistors would be a maximum at the nominal value. This may not be the case because manufacturers often select resistors from a given production lot for 5, 10, and 20 percent tolerances. Thus, if one orders resistors with a ± 10 percent tolerance, he may find very few within 5 percent of the nominal value.

Although composition resistors have notable limitations, they are widely used because of their low price and ready availability. In addition, they are relatively reliable when used properly. A list best summarizes the characteristics of composition resistors.

Noise : Poor

Stability : Poor

Reliability : Fairly Good

Temperature Coefficient : Poor

Moisture Characteristics : Poor

Voltage Coefficient : Poor

High-Frequency Characteristics : Fairly Good

Price and Availability : Attractive

Fixed-film resistors are superior to composition resistors in almost every respect. Composition resistors, however, have an advantage in price, availability, and sometimes size for the same wattage rating. Fixed-film resistors, which are available with a tolerance of ± 1 percent, are most often used where high stability is required. One can purchase film resistors with practically zero temperature coefficient of resistance. In military equipment, film resistors with a temperature coefficient of ± 50 PPM/ $^{\circ}\text{C}$ (parts per million per degree centigrade) are frequently used. Even though film resistors are quite stable in comparison to composition resistors, one would still expect 1-percent film resistors to vary from the nominal value by 3 to 5 percent over a period of one year. In some cases, much of the variation is caused by the effects of moisture. Where high stability is required, one should derate film resistors (to one-half the published power rating or less) and handle them with care particularly when soldering into a circuit.

Deposited carbon and metal film resistors are two common types of fixed-film resistors. The published (typical) characteristics of a given metal film resistor are listed in Table 4-3.

Table 4-3 Characteristics -- Metal Film Resistor

Minimum Available Tolerance	± 0.1%
Temperature Coefficient	± 15 PPM/ ° C
Voltage Coefficient	± 3 PPM/V
Noise	Equivalent to wirewound
Frequency	Good to at least 10 Mc
Wattage Rating	No derating to 100 ° C
Moisture	0.02%

Fixed-film resistors can be obtained with characteristics differing markedly from those in Table 4-3, and one should consult the manufacturer's specification sheets for design purposes.

Wirewound resistors are well suited for low-resistance, high-wattage applications. Internally-generated noise is extremely low in this type of resistor, and they can, therefore, be specified for use in low-noise circuits. Wirewound resistors are quite stable and reliable if properly constructed. The reliability of high-value wirewound resistors is somewhat questionable because the diameter of the resistance wire is decreased to a point where the resistor becomes susceptible to mechanical damage. Inductive effects of wirewound resistors limit their use to low- and medium-frequency applications.

It can be mentioned in passing that there are also several different types of potentiometers. These components can be obtained with single turn, multi-turn, composition material, wirewound, etc. Most of the considerations which apply to resistors also apply to potentiometers. In addition, one may also be concerned with end resistance, wiper shift, and linearity. There is a considerable difference in potentiometers, and one is advised to consult the manufacturer's specification sheets for anything other than a routine application.

4-2 CAPACITORS

A capacitor consists essentially of two conducting plates which are separated by an insulating or dielectric material. Such a definition is valid, but the Circuit Design Engineer is

concerned with more than the definition. He must know what to expect from a particular capacitor when it is connected into his circuit. The problem would be minimized if the various characteristics of all capacitors, regardless of type, were the same. However, the characteristics of the capacitor types are different, and no type is superior to the rest for every application. When a Circuit Designer specifies the value of a capacitor, he has not finished the problem. The type must be specified based upon the designer's judgment of his requirement. Other considerations besides value include dielectric material, voltage rating, temperature requirement, leakage current, reliability, size, cost, and availability.

A partial list according to dielectric material of capacitor types is composed of air, paper, mylar, polystyrene, mica, teflon, ceramic, and tantalum oxide. It is the purpose of this section to describe the properties of capacitors which are pertinent to application problems.

Very high discharge currents flow when charged capacitors are shorted. Repeated shorts can damage a capacitor, and it is, therefore, good practice to discharge a capacitor through some finite impedance. In connection with charged capacitors, it should be noted that they can be dangerous to personnel because of their low inherent internal impedance and high surge-current capability. An interesting fact is that a charged capacitor can be shorted, and yet a voltage will be present across the capacitor after the short is removed. This is due to the phenomenon of dielectric absorption. One may have to short the capacitor several times to eliminate the residual voltage. This particular effect is important in analog computers and integrating amplifiers. The magnitude of the residual voltage depends, among other things, on the type of dielectric material.

Another point which is applicable to most capacitors concerns the method of mounting them. The capacitance of a particular capacitor can be affected by pressure on the case. Tight-fitting clamps have caused catastrophic capacitor failures, and such methods of mounting should be employed only with considerable care.

Paper capacitors are characterized by low cost and ready availability, and they are applicable to most ordinary circuit requirements. Limitations of this type of capacitor include moisture susceptibility unless sealed, and relatively poor stability. Published data sheets for a particular metallized paper capacitor indicate a ± 10 percent change in capacitance for a temperature variation of from -55°C to 125°C . The manufacturer specifies no voltage derating up to an ambient temperature of 125°C , but a designer would typically derate anyway

for reliability reasons. Other specifications for this capacitor include a dissipation factor of less than 2 percent at 25°C and insulation resistance of 1,000 M Ω times microfarads at 25°C and at a voltage rating of 200 vdc. According to the specification, the insulation resistance need not exceed 3,000 M Ω . Standard tolerances for this type are ± 5 , ± 10 , and ± 20 percent. Other types are available also with tolerances of ± 1 , ± 2 , and ± 3 percent. Of course, a capacitor with a 1 percent tolerance will cost considerably more than the same capacitor with a 20-percent tolerance.

The stability of a capacitor is *not* defined by the tolerance. That is, 1-percent capacitors are not more stable than 20-percent capacitors if they are identical in every respect except tolerance. One applies a tolerance specification to limit the variations in nominal value from capacitor to capacitor at specified test conditions which usually include temperature (25°C) and frequency (60 cps or 1,000 cps).

It should be mentioned also that the ac voltage rating may differ from the dc voltage rating. For instance, the rms voltage rating of a given wax-impregnated metallized paper capacitor is 60 percent of the dc rating at 60 cps and 35 percent at 400 cps.

Polystyrene capacitors are often used in analog computers and timing circuitry because of their stable characteristics. The typical temperature coefficient of capacitance is negative and linear over the operating temperature range which is specified as -55°C to 65°C. These units are usable at ambient temperatures to 85°C if the voltage is derated to 60 percent of the nominal rating. A typical specification sheet for a polystyrene capacitor may include the following:

1. Temperature Coefficient	-100 PPM/°C
2. Long-Term Stability	0.1% per year
3. Dissipation Factor	Less than 0.1%
4. Insulation Resistance	500,000 M Ω
5. Dielectric Absorption	

Recovery voltage shall not exceed 0.5%
of applied voltage under specified conditions.

Standard tolerances for this type capacitor are ± 20 , ± 10 , ± 5 , ± 3 , ± 2 , and ± 1 percent.

Polystyrene capacitors are quite useful for applications requiring high stability over a moderate temperature range. Other types such as metallized-polycarbonate and plastic-film are used for the same applications (RC timers, integrators, etc.) when the temperature requirements are more severe. Both the metallized-polycarbonate and plastic-film capacitors are usable at ambient temperatures to 125°C without voltage derating. However, a designer would probably derate for reliability reasons, anyway.

A capacitor with a 600-V rating is physically larger than the same type of capacitor with say a 200-V rating, and, in addition, there may be a difference in price. These factors tend to restrain the Circuit Designer from "over" designing.

Metallized polycarbonate capacitors can be obtained with approximately the same magnitude of temperature coefficient of capacitance as polystyrene capacitors. Since in the case of polycarbonate the coefficient is positive and in the case of polystyrene the coefficient is negative, one can use the two types in conjunction to obtain a resultant capacitor which is quite stable for variations in temperature. Over a limited temperature range, plastic-film capacitors possess excellent stability characteristics. Typically, one might expect a ± 0.1 -percent variation in capacitance for a temperature variation of from 5°C to 65°C. The temperature coefficient of plastic-film capacitors versus temperature is not a linear relationship, and typical capacitors vary from the 25°C value by approximately +1 percent at 125°C and -1 percent at -55°C. Polystyrene, polycarbonate, and plastic-film capacitors are available in standard values of from approximately 0.001 μF to 5 μF .

Silver-mica capacitors are used in applications which require stable low-value capacitors. This type of capacitor is available in values of from 1 pF to approximately 30,000 pF. Standard tolerances are specified as low as ± 1 percent. A typical temperature coefficient for silver-mica capacitors is ± 100 PPM/°C (.01 percent per degree centigrade), and designated types can be used over a temperature range of from -55°C to 150°C.

Tantalum capacitors are characterized by very high capacity to unit volume ratio, and they are widely used for bypass and filter applications. Also, they are frequently used in time-delay circuits to generate time-delay intervals up to several hundred seconds. Possibly the two most severe limitations of tantalum capacitors are high leakage currents and poor stability. Life expectancy of from 5 to 10 years can be expected if the capacitors are used properly. It is an interesting fact that tantalum capacitors are more reliable when operated near their voltage

rating (say 10 percent of rating). The value of a given capacitor can vary markedly for changes in frequency and dc polarizing voltage, particularly at voltages much less than the rated voltage. There is some inductance associated with every type, and tantalum capacitors are poor in this respect. The impedance of a given 35- μ F capacitor is a minimum at about 200 kc, and the impedance increases at frequencies greater than 200 kc. Thus, the equivalent impedance becomes inductive at high frequencies.

Leakage current in a tantalum capacitor is appreciable and increases as either the voltage across the capacitor is increased or as the ambient temperature is increased. Equation (4-1) is used to describe, at least approximately, how much leakage current to expect from a plain-foil type tantalum capacitor

$$I = kCE \quad \mu A \quad (4-1)$$

where

I is maximum leakage current (μA)

k is a constant

0.02 at 25°C

0.20 at 85°C

0.25 at 125°C

C is in microfarads

E is in volts

One can refer to the manufacturer's specification sheets for final design figures, but Eq. (4-1) is useful for preliminary calculations.

Tantalum capacitors possess an appreciable temperature coefficient of capacitance. It is not feasible to list a typical temperature coefficient because this parameter varies markedly from one type of tantalum capacitor to another. The value of an etched-foil capacitor may vary from the room temperature value by -40 percent at -50°C and by +75 percent at +125°C, whereas a plain-foil capacitor under the same conditions would vary -35 percent and +25 percent, respectively. Other types are available which vary in capacitance less than ± 15 percent over a temperature range of from -80°C to 125°C.

Polarized tantalum capacitors should not be subjected to reverse voltages greater than 0.5 V. Non-polarized types are available for bipolar operation. In either case, ac ripple voltages should not exceed recommended values. The sum of the applied dc voltage and the peak ac ripple voltage should not exceed the rated dc working voltage.

Tantalum capacitors are available in a wide range of values including but not limited to $0.22\ \mu\text{F}$ to $330\ \mu\text{F}$. Available tolerances include ± 5 , ± 10 , and ± 20 percent.

4-3 INDUCTORS AND RELAYS

When a designer specifies an inductor, he may be required to specify not only the value of inductance but also such other parameters as coil Q , dc winding resistance, dc current through the inductor under operating conditions, mechanical configuration, and core type. There are many different types of inductors which are manufactured to satisfy various requirements. A partial list of inductor types includes ferrite core RF chokes, iron core RF chokes, adjustable ceramic RF inductors, toroidal inductors, and iron-core filter reactors.

Inductors which are designed for RF filter applications are small in value and physical size. These units may be purchased in values from $0.15\ \mu\text{H}$ to several mH. Toroidal inductors often feature high Q over a wide frequency range and minimum pickup from external magnetic fields. These inductors are available in a tolerance of ± 1 percent, and they maintain good stability over a wide temperature range (-55°C to 85°C). The approximate range of readily available values is 1 millihenry to several henries.

The inductance of a given inductor can vary widely with changes of dc current, and, in fact, some types are designed for a variation of inductance as a function of dc current. Such units are referred to as *swinging reactors*. A typical swinging reactor may vary in inductance from 25 H to 5 H as the inductor dc current is varied from 20 ma to 200 ma. In other applications, it is undesirable for inductance to vary as a function of dc current, and limitations on the inductance change with current are imposed by specification requirements. The dc current is sometimes specified at the point where there is a 5-percent change in inductance, and this is an indication to the Circuit Designer that the particular inductor should not, in general, be used at higher dc current levels.

To further illustrate the importance of dc current in specifying an inductor, the specifications of two filter reactors are compared. The first filter reactor is a 2-H inductor with a dc resistance of $160\ \Omega$, a dc current rating of 55 ma, and a weight of 0.25 lb. The second filter reactor is a 2-H inductor with a dc resistance of $47\ \Omega$, a dc current rating of 300 mA, and a weight of 3.25 lb. There is a direct correlation between weight or volume of core material (iron) and inductor dc current

capability. The basic constraint on allowable dc current involves the magnetic saturation characteristics of the core material.

Relays

Relays are ideally suited for certain switching and logic applications. The contact resistance (switch-closed impedance) is $0.1\ \Omega$ or less, and the switch-open impedance is many megohms. Thus, the characteristics of an ideal switch are closely approximated by relay contacts.

There are many different types of relays, and one should consult a manufacturer's catalog before selecting a relay for a given application. However, it is advisable for a Circuit Designer to be aware of the most common relay types. The standard coil voltage for military applications is 26.5 V, but relays are readily available with coil voltage ratings from approximately 1 V to 100 V. The corresponding coil dc resistance range is approximately $20\ \Omega$ to $10\ \text{k}\Omega$.

A relay with a rated coil voltage of 26.5 V dc is usually required by specification to actuate at a voltage less than the rated voltage. For instance, the pull-in voltage of a relay with a nominal coil rating of 26.5 V may be specified as 13 V maximum. This means that the relay is required to actuate when 13 V is applied across its coil. The dropout voltage is usually specified also, and the specification for the aforementioned relay is 2.3 V. This means that the activated relay must dropout or deactivate if the voltage across the coil decreases below 2.3 V. These specifications apply at an ambient temperature of 25°C . Since coil resistance is a function of temperature, the pull-in and dropout voltages vary as the coil temperature varies. At an ambient temperature of 125°C , the maximum pull-in voltage is specified at 18 V (versus 13 V at 25°C), and the dropout voltage is specified at 3.2 V (versus 2.3 V at 25°C). It should be noted that, although a relay is required to actuate at voltages considerably below the rated voltage, it is best to operate the relay at rated voltage because relays are more susceptible to vibration when operated at reduced voltages.

Standard contact arrangements include 2PDT (two-pole, double-throw), 4PDT, and 6PDT. Contact current rating depends upon the relay type, but standard contact ratings for relays that are used in military equipment include 2, 5, and 10 A resistive. The inductive current rating is usually one-half of the resistive rating. That is, a contact with a resistive current rating of 2 A will be rated for 1 A inductive. Derating for inductive current is necessary because the inductive kickback

voltage tends to arc across the contacts when the circuit is broken, and repeated arcing can damage the contacts.

There may, in fact, be several henries of inductance associated with a relay coil, and the switch which is used to activate and deactivate the relay must be protected from inductive kickback voltages just as the relay contacts themselves must be protected or used within their ratings. A transistor is often used as a switch to control a relay, and, in such cases, one must be even more careful to protect the transistor than if a mechanical switch were used. The most common method of protecting a transistor relay driver from inductive kickback voltages is to connect a diode in parallel with the relay coil with the anode of the diode connected to the low-voltage side of the relay coil. A disadvantage of this method, in addition to the requirement of an extra part, is the effect upon the relay dropout or deactivate characteristics. Dropout time will increase by a considerable percentage when a diode is connected in parallel with the relay coil. Normal dropout time (contact release time) is specified and is usually 5 ms or less. Contact operate time is also usually 5 ms or less. It should be noted that the contact operate time increases as the coil-energizing voltage is reduced. In other words, a relay will operate faster when full rated voltage is applied rather than, say, the minimum pickup voltage.

Standard 26.5-V dc relays have a coil dc resistance of 500 to 600 Ω , but sensitive relays are available which require very little operating power (several thousand ohms of coil resistance). Sensitive relays are often considered less reliable than standard relays when used in a high vibration environment. Other types of relays include latching relays and time-delay relays. Time-delay relays may be either the thermal type or the electronic type. In the electronic type, the delay period is generated electronically, and a standard relay is activated at the end of the time-delay period.

Since they possess two stable states, latching relays can be used as flip-flops. A momentary signal will cause a latching relay to change state, and the relay will hold the new state after the input signal is removed. Thus, a latching relay requires no holding power.

4-4 TRANSFORMERS

The usefulness of transformers as circuit elements is sometimes not fully appreciated until one is restricted in using them for reasons such as size, weight, and stray magnetic

fields. Such requirements are frequently imposed on circuitry for satellite applications. However, in other areas, transformers are virtually indispensable. Primary uses of transformers include power transmission, power conversion, voltage or current amplification by a fixed number (which may be greater than or less than unity), and ac coupling between amplifier stages.

Transformers are available with characteristics which closely approximate the characteristics of ideal transformers. A designer can often assume that the transformer-exciting current is negligible, that the output power is equal to the input power (efficiency of 100 percent), and that the internal impedance is equal to zero so that the transformer regulation characteristics are ideal. In other cases, the designer cannot assume that any of the foregoing conditions are true; it depends on the particular transformer type and the particular application.

To specify a transformer properly, the designer must be familiar with the characteristics of available transformers. Parameters which are usually specified by the manufacturer include turns ratio, power level, nominal primary and secondary voltages, allowable primary dc current, primary and secondary impedances, frequency response, and primary and/or secondary dc winding resistance. The specified characteristics of a given transformer will usually not include all of the aforementioned parameters. Only the characteristics which are pertinent to a particular application are specified. The manufacturer will indicate an intended application for his product. Typical applications include power, interstage, plate-to-grid, input, output, isolation, transistor, filament, etc.

Transformers may have multiple secondaries, and the turns ratio from the primary to each secondary is given. For instance, a transformer with a specified turns ratio of 1:2 CT will transform 1 V on its primary to 2 V across the whole secondary with 1 V between either end of the secondary and the center tap. The voltage from the center tap to one side of the secondary is 180° out of phase with the voltage from the center tap to the other side of the secondary. Push-pull driver amplifiers are easily mechanized with transformers because signals with equal amplitudes and opposite phase can be obtained from transformers with center-tapped primaries and/or secondaries.

There is a direct correlation between power rating and weight of a transformer. When one specifies power, one in effect specifies transformer weight, too, assuming a given core material and no other stringent requirements such as low distortion and high efficiency. Requirements such as low distortion and high efficiency tend to increase transformer size and weight.

Primary and secondary voltage levels are indicated as nominal values, and most transformers can be operated at other voltage levels. However, other specifications such as efficiency, distortion, and regulation apply at rated voltage or current conditions.

For many applications, it is sufficient to compute transformer regulation from the dc winding resistances. The error involved with this technique is often negligible in cases where one is interested in transformer regulation. Assume a transformer turns ratio of 1:2, a primary dc winding resistance of $10\ \Omega$, and a secondary dc winding resistance of $20\ \Omega$. The primary resistance is transformed into the secondary by the square of the turns ratio, or $40\ \Omega$ in this case. This resistance is added to the secondary resistance, and the total resistance is $60\ \Omega$. Thus, the simplified equivalent circuit of the transformer is a voltage generator with a magnitude of twice the primary signal voltage and an output resistance of $60\ \Omega$. From this equivalent circuit one can easily compute the no-load to full-load regulation of the transformer. The percent regulation is equal to 100 times the quantity no-load voltage minus full-load voltage divided by the full-load voltage.

When an impedance ratio is specified for a transformer, an intended application is indicated for optimum utilization of the transformer. The transformer regulation characteristics, dc winding resistances, and output impedance are *not* defined by the impedance ratio. For instance, a transformer with a primary-to-secondary impedance ratio of $1,000\ \Omega$ to $50,000\ \Omega$ is a transformer which has been designed to operate from a signal generating source with an output impedance of $1,000\ \Omega$ and into a secondary impedance of $50,000\ \Omega$. Although the specified impedances are optimum for the given transformer, one can use the transformer with other impedances if maximum voltage and power ratings are not exceeded.

An interesting point is involved in the explanation of why impedances are transformed across a transformer by the square of the turns ratio rather than directly as the turns ratio. If one assumes that the transformer efficiency is 100 percent, then the output power is equal to the input power, and the following calculation is to determine the relationship between primary and secondary impedances

$$e_p i_p = e_s i_s$$

$$e_p \frac{e_p}{Z_p} = e_s \frac{e_s}{Z_s}$$

$$\frac{e_p^2}{Z_p} = \frac{ne_p^2}{Z_s}$$

$$\frac{1}{Z_p} = \frac{n^2}{Z_s}$$

$$Z_s = n^2 Z_p \quad \Omega$$

The result indicates that an impedance in the primary is transformed by the square of the turns ratio into the secondary.

4-5 SEMICONDUCTOR DIODES

A semiconductor diode is a unidirectional switch with, ideally, zero impedance in one direction and infinite impedance in the opposite direction. Applications for diodes are varied, including logic and computer circuitry. Rectifiers are high-current, high-wattage diodes and are used in power supplies and other power applications.

The characteristics of diodes which are usually defined by the manufacturer include maximum reverse-voltage rating, maximum average-forward current, minimum current at a forward voltage drop of 1 V, maximum reverse-leakage current at a specified reverse voltage and temperature, maximum allowable one-cycle (60 cps) surge current, and recovery characteristics. The manufacturer usually includes in the data sheet a curve of forward current versus forward voltage. A typical curve for a silicon diode is indicated in Fig. 4-4.

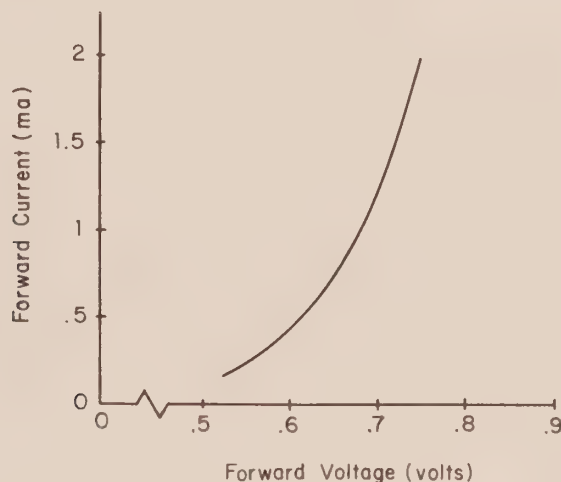


FIG. 4-4 Diode Characteristic

The region of the curve near the origin is not normally specified, but very little current will flow through the diode if the forward voltage is less than $1/2$ V. In fact, semiconductor diodes can be used at low forward voltages (less than $1/2$ V for silicon and $1/10$ V for germanium) in a manner similar to Zener diodes. That is, silicon diodes conduct very little current if the forward voltage is less than $1/2$ V, and they conduct appreciable current if the forward voltage is greater than $1/2$ V. The corresponding number for germanium diodes is 0.1 to 0.15 V.

There is a temperature coefficient associated with the forward voltage drop of semiconductor diodes. The coefficient is approximately -2 mV per degree centigrade rise in junction temperature. Reverse-leakage current is also temperature-dependent, and one should consult the manufacturer's data sheets for design purposes.

An interesting fact is that the forward impedance of a diode which is operated at voltages near zero volts is virtually the same as the reverse impedance. In other words, the magnitude of current flow through the diode is essentially the same if the voltage across the diode is, say, $+0.1$ V or -0.1 V (for silicon). Appreciable reverse voltage is necessary before a diode attains its true reverse impedance.

If reverse voltage is suddenly applied to a diode which is conducting current, some time will elapse before the diode recovers to its high impedance state. The recovery time is proportional to the magnitude of forward current and inversely proportional to the magnitude of the applied reverse voltage. The reverse recovery characteristic of a particular silicon switching computer diode is specified as follows: The diode shall recover to a minimum reverse resistance of $400\text{ k}\Omega$ in a maximum time of $1\text{ }\mu\text{s}$ when switched from 30 ma of forward current to a reverse voltage of 35 V.

Diodes are designed for several different applications such as high-speed switching circuits, low reverse leakage, high conductance, and general purpose. Of course, rectifiers are designed for high current and high power applications. Switching diodes should have good reverse recovery characteristics, relatively low-reverse-leakage current, and fairly good conductance characteristics. High-conductance diodes are designed to conduct high current at low forward voltages. Low-reverse-leakage diodes are designed for applications which require very high reverse impedance.

Zener Diodes

At some reverse voltage all diodes break down and conduct current in the reverse direction. After the breakdown voltage has

been reached, a diode conducts appreciable current for very little increase in reverse voltage. If the reverse current is limited such that the power dissipated in the diode is insufficient to destroy it, one can use the diode in a manner similar to the application of voltage-regulating tubes. However, standard diodes are not designed to have controlled reverse-breakdown characteristics; Zener diodes are designed for operation in the reverse-breakdown mode. The reverse-current-vs.-reverse-voltage curve of a Zener diode depicts a breakpoint or knee which is much better defined and more abrupt than equivalent curves of standard diodes. Furthermore, dynamic impedance in the breakdown region is less for Zener diodes. That is, the reverse voltage across a Zener diode changes very little for a considerable change in reverse current.

Zener diodes are readily available with nominal Zener voltage ratings of from approximately 2.5 V to 200 V and power ratings of from 0.25 W to 50 W. Higher wattage units must be mechanically connected to a heat sink to prevent excessively high junction temperatures. Standard tolerances on Zener voltage ratings include 5, 10, and 20 percent.

There is a temperature coefficient associated with the Zener voltage rating which is appreciable, especially with high-voltage Zener diodes. However, temperature-compensated reference diodes are available which are quite stable. Type numbers can be specified with various voltage-temperature coefficients including 0.01, 0.005, 0.002, 0.001, and 0.0005 percent per degree centigrade. Some of these units are designed to operate in a temperature range of from -55°C to 150°C .

4-6 DESIGN EXAMPLE

The input and output characteristics of a certain black box are specified as follows: There are two input signals and one output signal. One input signal is a 400-cps, 26-V sinusoidal voltage, and the other input signal is a control voltage which is either 0 or 28 Vdc. The output signal is to be sinusoidal and 5 V or greater in magnitude. The phase of the output voltage with respect to the ac input voltage is to be -45° if the control signal is 0 V and -90° if the control signal is 28 V. The steady-state value of the output voltage shall not change by more than 10 percent when the control signal changes state. The input impedance to the ac signal shall be greater than $10\text{ k}\Omega$ in magnitude, and the output impedance shall be less than $20\text{ k}\Omega$ in magnitude. The input impedance to the dc control signal shall be greater than $300\text{ }\Omega$.

Ambient temperature is specified as -20°C to 85°C . The initial tolerance in regard to the phase specification of each output signal is ± 5 percent, but the variation in phase over the specified temperature range shall be less than ± 1 percent.

The problem is to design a circuit to replace the black box, and the selected method of satisfying the design assignment is indicated in Fig. 4-5.

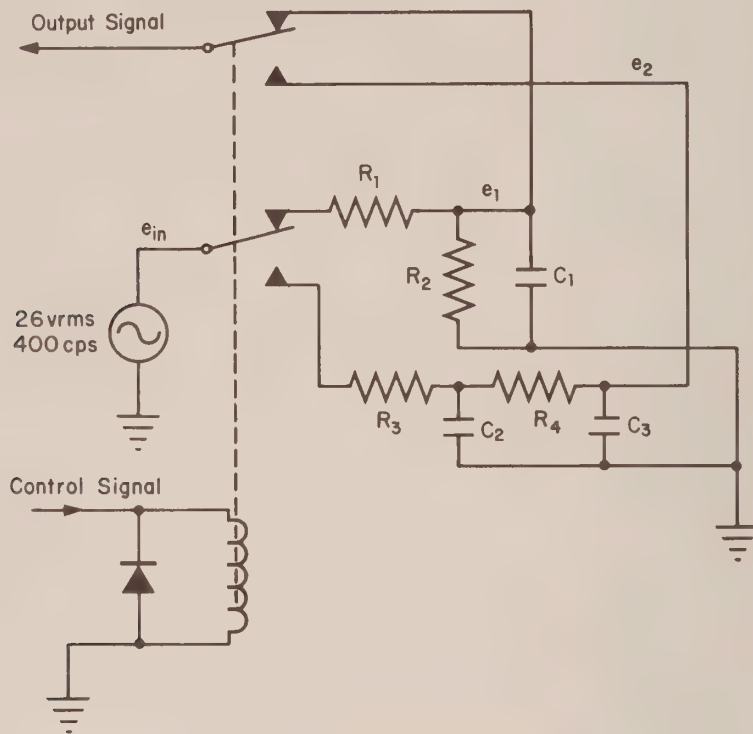


FIG. 4-5 Design Example

The 90° phase shift circuit is composed of resistors R_3 and R_4 and capacitors C_2 and C_3 . It is logical to design the circuit so that there will be 45° of phase shift across each section. Because of the specified requirements, it is desirable that resistor R_3 be of the order of $10\text{ k}\Omega$. In a single section, the capacitive reactance is equal in magnitude to the resistance when the phase shift is 45° . A standard capacitor value is $0.033\text{ }\mu\text{F}$, and the reactance of such a unit at 400 cps is approximately $12.1\text{ k}\Omega$. Furthermore, standard 1-percent resistors can be obtained with a value of $12.1\text{ k}\Omega$. Therefore, let resistors R_3 and R_4 be equal to $12.1\text{ k}\Omega$, and capacitors C_2 and C_3 be equal to $0.033\text{ }\mu\text{F}$.

In a two-section circuit where the resistors are equal and the capacitors are equal, the total phase shift is equally divided between the two sections. Under similar conditions, the phase shift is not equally divided when the number of sections exceeds

two. The transfer function of the two-section circuit is as follows:

$$\frac{e_2}{e_{in}} = \frac{-X^2}{R^2 - j3RX - X^2}$$

Since the design is for 45° of phase shift per section, the magnitude of X is set equal to the magnitude of R with the following result:

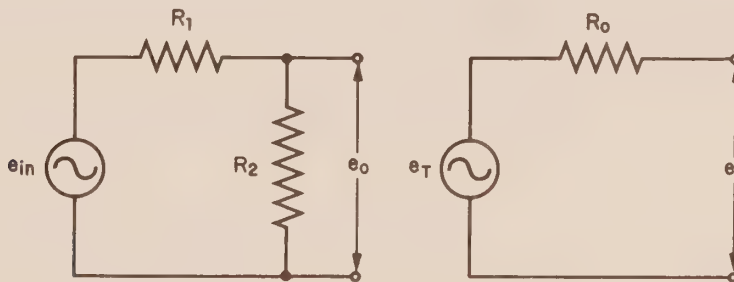
$$\frac{e_2}{e_{in}} = 0.333 \angle -90^\circ$$

The attenuation factor of the two-section circuit is 0.333. The design values for this circuit are:

$$R_3 = R_4 = 12.1 \text{ k}\Omega$$

$$C_2 = C_3 = 0.033 \text{ }\mu\text{F}$$

The single-section circuit is to produce 45° of phase shift with a nominal attenuation factor of 0.333 (because of the requirement for less than 10 percent change in output when the control signal is switched from one state to the other state). Normally, the attenuation factor of a single 45° section would be 0.707. That is, the output amplitude would be 70.7 percent of the input amplitude. Resistor R_2 is included to yield a total attenuation factor of 0.333. The next step is to compute the ratio of R_1 to R_2 . Thévenin's Theorem is applicable to this problem.



Original Circuit

Thévenin Equivalent

The desired value of e_T with respect to e_{in} is found as follows:

$$\frac{e_{in}}{e_T} = \frac{.707}{.333} = 2.12$$

The relationship of R_1 and R_2 can be determined to give the

proper voltage division

$$e_T = \frac{e_{in}}{2.12} = \frac{R_2 e_{in}}{R_1 + R_2}$$

$$R_1 = 1.12 R_2$$

If the value of capacitor C_1 is to be equal to the value of the other capacitors ($.033 \mu\text{F}$), then the parallel impedance of resistors R_1 and R_2 must be equal to $12.1 \text{ k}\Omega$. That is, the Thévenin output impedance R_o must be equal to $12.1 \text{ k}\Omega$.

$$\frac{R_1 R_2}{R_1 + R_2} = 12.1 \text{ K}$$

Substituting $R_1 = 1.12 R_2$

$$\frac{1.12 R_2}{2.12} = 12.1 \text{ K}$$

$$R_2 = 22.9 \text{ k}\Omega$$

$$R_1 = 25.6 \text{ k}\Omega$$

Standard 1 percent values are $25.5 \text{ k}\Omega$ and $22.6 \text{ k}\Omega$. Therefore, the following values are specified

$$R_1 = 25.5 \text{ k}\Omega$$

$$R_2 = 22.6 \text{ k}\Omega$$

$$C_1 = 0.033 \mu\text{F}$$

The transfer function of both output signals can now be written assuming that these signals are not loaded by an external impedance

$$e_1 = 0.333 E_{in} \angle -45^\circ = 8.67 \angle -45^\circ \text{ V}$$

$$e_2 = 0.333 E_{in} \angle -90^\circ = 8.67 \angle -90^\circ \text{ V}$$

The design task has not yet been completed because the components have not been fully specified. The specified phase shift tolerance was ± 5 percent, and both the capacitors and resistors are available with a tolerance of ± 1 percent. However, the cost of a stable capacitor with a tolerance of 1 percent is not negligible, and a significant saving can be realized if a tolerance of 3 percent is specified.

The temperature coefficient of the RC product has to be such that the phase shift varies less than 1 percent over the specified temperature range (-20°C to 85°C). An analysis of component data indicates that a combination of metal-film resistors and plastic-film capacitors will be suitable for this application from a stability standpoint. It should be noted that the designer is not necessarily limited to these particular types.

The requirements pertaining to the relay and protective diode are not stringent, and these components are specified quite easily. The relay can be a standard 2PDT, 26.5-V relay. The reverse voltage rating of the diode must exceed the peak value of the control signal, and the peak current required from the diode is the relay dc coil current. Average diode current is essentially equal to zero.

The component specifications are summarized below:

Resistors:	$R_1 = 25.5K \pm 1\%$	Metal Film
	$R_2 = 22.6K \pm 1\%$	Metal Film
	$R_3 = 12.1K \pm 1\%$	Metal Film
	$R_4 = 12.1K \pm 1\%$	Metal Film

Capacitors: All— $0.033 \mu\text{F} \pm 3\%$ Plastic Film

Relay: 26.5-V, 2PDT

Diode: General Purpose Silicon (1N645)

PROBLEMS

- 4-1 A bias voltage is required at a magnitude of 700 mV dc. The output current requirement is 0 to 100 μ A. The available voltage source is a battery with an output voltage of 28 ± 4 V. The tolerance associated with the 700-mV bias signal is ± 10 percent. Design a circuit, assuming room temperature operation to obtain the desired bias voltage.
- 4-2 In the circuit of Fig. 1, the capacitor is a 1- μ F, 35-V, polarized tantalum type.
- What is the steady-state value of the output voltage at an ambient temperature of 25°C? Assume that the leakage current is at a maximum.
 - What is the steady-state value of the output voltage at an ambient temperature of 85°C?

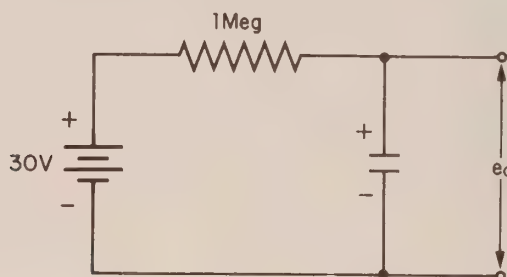


FIG. 1 Capacitor Leakage Problem

- 4-3 A 1-V sinusoidal signal is impressed across the primary winding of a one-to-two step-up transformer. The primary dc winding resistance is 100 Ω , and the secondary winding resistance is 200 Ω . A 1.8-k Ω load resistor is connected across the secondary terminals. Determine, approximately, the voltage across the load resistor.
- 4-4 A temperature-sensitive bias voltage at an approximate magnitude of 300 mV is required. The desired temperature characteristic is -1 mV/C, and the small signal output impedance must be $10\text{ k} \pm 3\%$ Ω . The available supply voltage is 30 vdc. Design a circuit to satisfy the requirement.
- 4-5 Overvoltage and undervoltage protection must be supplied for certain equipment which operates on 28 vdc and which

draws 4 A of current. Voltage is to be removed from this equipment if the supply voltage exceeds 34 vdc or decreases below 20 vdc. Assuming room ambient conditions, design a circuit to satisfy the requirements.

- 4-6 An LC filter is to be designed to derive a dc supply voltage from a 26-vrms, 400-cps sinusoidal voltage. The 26-V signal is full-wave rectified (by ideal rectifiers) and applied to the input of the filter. The dc output current is 0.1 to 0.5 A, and the maximum allowable dc voltage drop across the inductor is 5 V. In addition, the output ripple voltage is specified as 25 mV rms, maximum. Design a single-section LC filter circuit to satisfy the requirements.
- 4-7 Seventy ms after the initiation of a step voltage, an output signal is required. The method of generating the delayed signal involves the design of a monostable multivibrator with a period of 70 ms. The multivibrator period is controlled essentially by one resistor and one capacitor and is defined as equal to $0.7 RC$. The tolerance associated with the period is ± 5 percent, the specified temperature range is -20°C to 65°C , and the period must not vary more than $\pm 1\%$ as a function of temperature. Other considerations limit the value of the resistor to a range of from $50\text{ k}\Omega$ to $250\text{ k}\Omega$. The supply voltage is 30 vdc. Design the RC portion of the multivibrator.

BIBLIOGRAPHY

- Allen-Bradley Electronic Components Catalog, Allen-Bradley Company.
- Electron Products Capacitor Catalog, Electron Products Company, Division of Marshall Industries.
- Henney, K. and C. Walsh: "Electronic Components Handbook," chaps. 3-5, McGraw-Hill Book Company, New York, 1957.
- Sprague Engineering Bulletin No. 3520D, Sprague Electric Company, North Adams, Mass., 1960.

5

EQUIVALENT CIRCUITS

5-1 VACUUM TUBE-TRIODE

For an active component to be useful as a circuit element, its characteristics must be fully defined. In particular, a mathematical description is necessary because the design of circuits is based on a mathematical model. Consider the problems associated with the application of a given element, such as a vacuum tube, if its characteristics are not defined. Quite obviously, the engineer must determine the appropriate device parameters before he can proceed. Furthermore, if the device is to be used in multiple and various applications, the definition must be general.

Thus, equivalent circuits have been devised to describe or define the characteristics of various active elements in terms of voltage generators, current generators, resistors, capacitors, etc. The engineer can then use one equivalent circuit for all vacuum tube triodes, one for all vacuum tube pentodes, etc. Although parameter values change from triode to triode, for instance, the equivalent circuit does not change (when expressed in general terms). However, a complete equivalent circuit is rather complicated and is not necessary for most applications. Therefore, there are separate equivalent circuits for dc, mid-frequency, and high-frequency operation.

It must be mentioned that all equivalent circuits are approximations to the actual device. This is partly true because the device parameters vary as a function of dc operating point, age, etc. In fact, it is unusual to find a parameter which is absolutely constant. Nevertheless, it is possible to design circuits successfully with approximate equivalent circuits.

The small-signal, mid-frequency, linear equivalent circuit of a vacuum tube triode is depicted in Fig. 5-1. Resistor R_1 is the grid leak resistor (which is external to the tube), resistor r_p is the plate resistance, and μ is the voltage amplification factor. Thus, the equivalent circuit is composed of an input resistor R_1 , a voltage generator with a magnitude of μ times the input voltage, and a series resistor r_p .

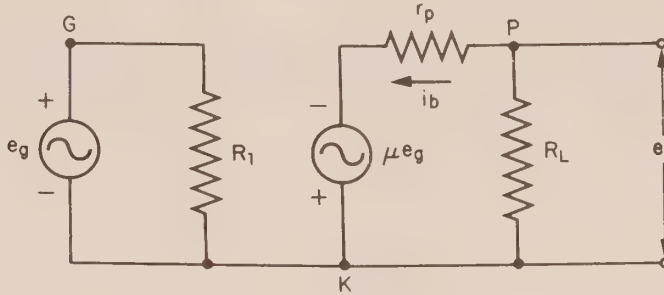


FIG. 5-1 Triode Equivalent Circuit

The Circuit Designer is usually interested in input impedance, output impedance, and voltage, current, and power gains. The input impedance is equal to the grid leak resistance R_1 , and the output impedance is equal to the parallel combination of r_p and R_L (the Thévenin output impedance)

$$R_o = \frac{r_p R_L}{r_p + R_L} \text{ ohms} \quad (5-1)$$

The voltage gain is calculated as follows where i_b is the plate current:

$$\begin{aligned} i_b &= \frac{\mu e_g}{r_p + R_L} \\ e_o &= -i_b R_L \\ &= \frac{-\mu e_g R_L}{r_p + R_L} \\ A_v &= \frac{e_o}{e_{in}} \\ &= \left(\frac{-\mu e_g R_L}{r_p + R_L} \right) \left(\frac{1}{e_g} \right) \end{aligned} \quad (5-2)$$

$$A_v = \frac{-\mu R_L}{r_p + R_L} \quad (5-2) \quad (\text{cont'd})$$

The minus sign in Eq. (5-2) indicates that the output signal is phase shifted 180° from the input signal.

One seldom calculates current gain in vacuum tube circuitry because the input current is negligibly small. The gain is, however, as follows:

$$\begin{aligned} A_i &= \frac{i_b}{i_{in}} \\ &= \frac{e_o/R_L}{e_g/R_1} \\ &= \frac{\mu R_L e_g/(r_p + R_L)(R_L)}{e_g/R_1} \\ A_i &= \frac{\mu R_1}{r_p + R_L} \end{aligned}$$

Power gain is equal to voltage gain multiplied by current gain

$$\begin{aligned} |A_p| &= A_v A_i \\ &= \left(\frac{\mu R_L}{r_p + R_L} \right) \left(\frac{\mu R_1}{r_p + R_L} \right) \\ A_p &= \left(R_1 R_L \right) \left(\frac{\mu}{r_p + R_L} \right)^2 \end{aligned}$$

Resistors r_p and R_L in Fig. 5-1 form a voltage divider where the output voltage is equal to the divider input voltage multiplied by $R_L/(r_p + R_L)$. The quantity $R_L/(r_p + R_L)$ is the attenuation factor of the network. This resistor combination functions in the same way as a gain control potentiometer. In fact, resistor dividers can be used to reduce gain as well as to reduce or attenuate voltages. The object of this discussion is to develop an easier means of deriving Eq. (5-2). In the circuit of Fig. 5-1, maximum voltage gain is equal to the amplification factor (when

R_L is equal to ∞). This maximum gain is reduced by the resistor divider r_p and R_L . As previously indicated, the reduction factor is equal to $R_L/(r_p + R_L)$. Therefore, the magnitude of the voltage gain is as follows:

$$|A_v| = \frac{\mu R_L}{r_p + R_L}$$

One then remembers that there is phase inversion between the input and output signals which requires multiplication of one side of the above equation by -1 . The result is Eq. (5-2).

Example 5-1 is used to illustrate calculations associated with triode amplifiers. It is important to realize that the magnitude of the voltage generator μe_g in Fig. 5-1 is always equal to the grid-to-cathode voltage multiplied by the amplification factor. In Fig. 5-1 the grid-to-cathode voltage is simply e_g .

Example 5-1

The assignment is to design an amplifier with voltage gain of approximately 10 to drive an $8.35\text{-K}\Omega$ ac load impedance. A tube type is selected with the following characteristics:

$$\mu = 20$$

$$r_p = 7,700 \quad \Omega$$

An examination of Eq. (5.2) indicates that the voltage gain will be approximately 10 if the total ac load impedance is equal to $7.5\text{ k}\Omega$. Therefore, a dc load resistance of 75 K is chosen which makes the total ac load impedance equal to $7.5\text{ k}\Omega$. The supply voltage is specified as 300 V , and Class A operation dictates a dc operating point of 150 V . One then refers to the plate characteristic curves of the particular tube to draw the appropriate dc load line. Two points establish the load line. One point is the supply voltage (300 V), and the other point is equal to the supply voltage divided by the dc load resistance (4 mA). For Class A operation, the dc operating point should be at a plate voltage of 150 V and a plate current of 2 mA . From the plate characteristic curves, a grid bias potential of -6 V is required at the indicated operating point. Since a negative supply voltage is not available, self bias must be used. That is, a resistor must be included in series with the cathode. Since the quiescent plate current is 2 mA and the required bias voltage is 6 V , the resistor value is $6/2$ or $3\text{ k}\Omega$. The proposed circuit is depicted in Fig. 5-2.

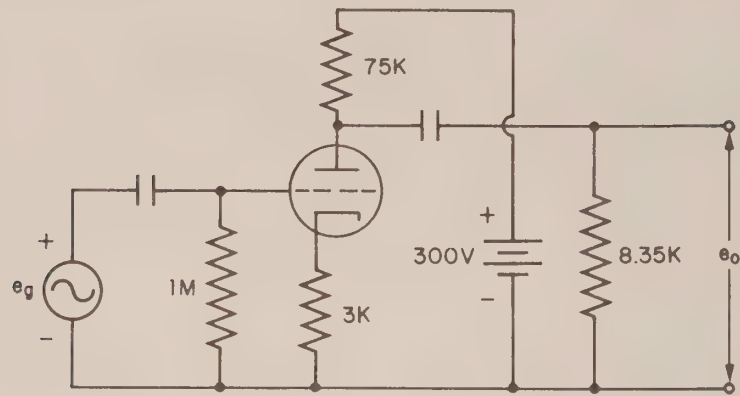


FIG. 5-2 Triode Amplifier

An equivalent circuit for the amplifier of Fig. 5-2 is drawn in Fig. 5-3

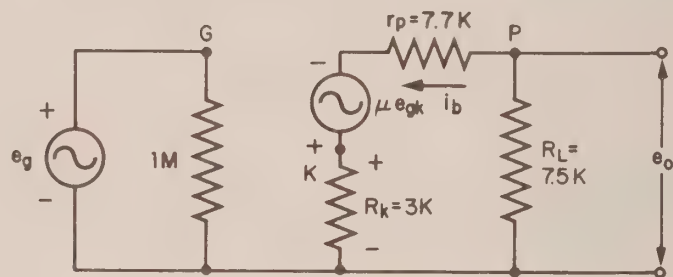


FIG. 5-3 Equivalent Circuit of Triode Amplifier

The voltage gain is calculated as follows:

$$e_o = -i_b R_L$$

$$e_{gk} = -i_b R_K + e_g$$

$$i_b = \frac{\mu e_{gk}}{r_p + R_K + R_L}$$

$$= \left(\frac{\mu}{r_p + R_K + R_L} \right) (e_g - i_b R_K)$$

Solving for i_b :

$$i_b = \frac{\mu e_g}{r_p + R_L + (\mu + 1) R_K}$$

Solving for the output voltage e_o :

$$\begin{aligned} e_o &= -i_b R_L \\ &= \frac{-\mu e_g R_L}{r_p + R_L + (\mu + 1) R_K} \end{aligned}$$

The voltage gain is then:

$$\begin{aligned} A_v &= \frac{e_o}{e_g} \\ A_v &= \frac{-\mu R_L}{r_p + R_L + (\mu + 1) R_K} \end{aligned} \quad (5-3)$$

Substituting numerical quantities:

$$\begin{aligned} A_v &= \frac{-(20)(7.5)}{7.7 + 7.5 + (21)(3)} \\ &\cong -1.9 \end{aligned}$$

The result differs considerably from the desired voltage gain of approximately 10 because the cathode resistor R_K introduces negative feedback, thereby decreasing the gain. The usual procedure is to connect a capacitor in parallel with the cathode resistor R_K where the capacitive reactance is much less, at the lowest frequency of interest, than the value of R_K . In such a case, resistor R_K is ac short-circuited and Eq. (5-3) reduces to Eq. (5-2). The voltage gain is then:

$$\begin{aligned} A_v &= \frac{-(20)(7.5)}{7.7 + 7.5} \\ &\cong -9.9 \end{aligned}$$

Interelectrode capacitances become significant at higher signal frequencies because the resulting reactances cause a reduction in gain and the introduction of phase shift. These capacitances are referred to as grid-cathode C_{gk} , grid-plate C_{gp} , and plate-cathode C_{pk} where the grid-plate capacitance is perhaps the most significant because it provides a direct feedback path from output to input. In fact, as the grid-to-cathode

voltage increases, the plate-to-cathode voltage decreases A_v times as much. Therefore, the voltage change across C_{gp} is many times as much as the equivalent voltage change across C_{gk} . The result is an effective multiplication of the grid-plate capacitance C_{gp} . Thus, the input capacitance of a triode amplifier may be significant even at moderate signal frequencies.

In the equivalent circuit of Fig. 5-1, the input capacitance is in parallel with the grid leak resistor R_1 . The magnitude of the capacitance C_{in} is found from Eq. (5-4) where A_v is defined by Eq. (5-2) (and is a negative quantity)

$$C_{in} = C_{gk} + (1 - A_v)(C_{gp}) \quad \mu\mu F \quad (5-4)$$

5-2 VACUUM TUBE-PENTODE

One significant difference between pentodes and triodes, aside from the two extra elements (screen grid and suppressor grid) associated with pentodes, is the much higher output impedance of the pentode.

Equivalent circuits are devised to approximate actual devices as nearly as possible, and one should not assume that all equivalent circuits are comprised of voltage generators. A theoretical constant voltage generator is a generator with an output *voltage* which is not a function of the load impedance; whereas, a theoretical constant current generator is a generator with an output *current* which is not a function of the load impedance. Furthermore, the output impedance of a theoretical voltage generator is zero, and the output impedance of a like current generator is infinite.

Because the output impedance of a pentode is relatively high, the equivalent circuit of a pentode contains a current generator as indicated by Fig. 5-4

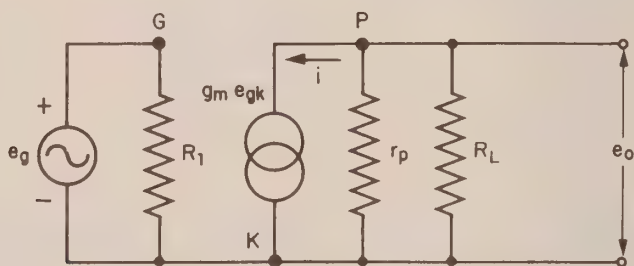


FIG. 5-4 Pentode Equivalent Circuit

The quantity g_m is the transconductance and is defined by Eq. (5-5)

$$\mu = g_m r_p \quad (5-5)$$

The output voltage e_o of Fig. 5-4 is equal to $-g_m e_{gk}$ multiplied by the parallel combination of r_p and R_L

$$e_o = - \left(g_m e_{gk} \right) \left(\frac{r_p R_L}{r_p + R_L} \right)$$

The voltage gain is then:

$$\begin{aligned} A_v &= \frac{e_o}{e_g} \\ &= \frac{e_o}{e_{gk}} \\ A_v &= \frac{-g_m r_p R_L}{r_p + R_L} \end{aligned} \tag{5-6}$$

Quite often the plate resistance r_p is much larger than R_L and Eq. (5-6) reduces to Eq. (5-7)

$$A_v \cong -g_m R_L \tag{5-7}$$

5-3 TRANSISTOR (T)

A number of equivalent circuits have been devised to describe the transistor. One reason for the multiplicity of circuits is the differing requirements of the device designer, the manufacturer, and the circuit engineer. The manufacturer, for instance, desires an equivalent circuit wherein he can measure easily and economically the various parameters associated with transistors. The circuit engineer desires, on the other hand, an equivalent circuit which can be readily analyzed by conventional circuit techniques and which is compatible with the external addition of resistors, capacitors, etc. The T equivalent circuit is perhaps most adaptable to the circuit engineer's requirements. However, the manufacturer prefers the hybrid or h equivalent circuit and usually specifies the device in terms of h parameters. Thus, the Circuit Designer should be familiar with at least two equivalent circuits.

In the consideration of transistors, current gain (h_{fe} or β) is an important factor whereas with vacuum tubes voltage

amplification (μ) is the corresponding factor. Such is the case because of inherent differences in the two devices. There is a relatively linear relationship between grid voltage variations and plate voltage variations. However, the corresponding base-collector voltage characteristic is quite nonlinear. The transistor input voltage (base-emitter) characteristic is, in fact, similar to that of a semiconductor diode; but the base current vs. collector current characteristic is relatively linear, and this relationship is used in the definition of transistor characteristics.

A significant assignment is to master prevalent transistor terminology. A partial list of the more important transistor parameters is found in Table 5-1.

Table 5-1

h_{FE}, B	Common emitter dc current gain.
h_{fe}, β	Common emitter small-signal current gain with output ac short-circuited.
h_{fb}, α	Common base small-signal current gain with output ac short-circuited.
h_{fc}	Common collector small-signal current gain with output ac short-circuited.
h_{ib}	Common base small-signal input impedance with output ac short-circuited.
h_{ie}	Common emitter small-signal input impedance with output ac short-circuited.
h_{ic}	Common collector small-signal input impedance with output ac short-circuited.
h_{ob}	Common base small-signal output admittance with input ac open-circuited.
h_{oe}	Common emitter small-signal output admittance with input ac open-circuited.
h_{oc}	Common collector small-signal output admittance with input ac open-circuited.
h_{rb}	Common base small-signal reverse voltage transfer ratio with input ac open-circuited.
h_{re}	Common emitter small-signal reverse voltage transfer ratio with input ac open-circuited.
h_{rc}	Common collector small-signal reverse voltage transfer ratio with input ac open-circuited.
f_{α}, f_{hfb}	Common base small-signal current gain cutoff frequency.
f_{β}, f_{hfe}	Common emitter small-signal current gain cutoff frequency.
f_{max}	Maximum frequency of oscillation.
f_t	Gain bandwidth product where h_{fe} equals 1.
I_{CBO}, I_{co}	Dc collector current where emitter is open-circuited (leakage current).

Table 5-1 (continued)

I_{CEO}	Dc collector current where base is open-circuited.
I_{CER}	Dc collector current where a resistor is connected from base to emitter.
I_{CES}	Dc collector current where the base is shorted to the emitter.
BV_{CBO}	Dc breakdown voltage collector to base with emitter open-circuited.
BV_{CEO}	Dc breakdown voltage collector to emitter with base open-circuited.
BV_{CER}	Dc breakdown voltage collector to emitter with a resistor connected from base to emitter.
BV_{CES}	Dc breakdown voltage collector to emitter with base shorted to emitter.
V_{BE}	Base-to-emitter voltage.
$V_{CE(sat)}$	Collector-to-emitter saturation voltage.
r_e	Small-signal emitter resistance.
r_b	Small-signal base resistance.
r_c	Small-signal collector resistance.
r_m	αr_c
r_d	$(1 - \alpha) r_c$
r_{sat}	Collector-to-emitter saturation resistance.
C_{ob}	Output capacitance.
C_c	Collector-to-base capacitance.
θ_{JC}	Thermal resistance junction to case ($^{\circ}\text{C}/\text{W}$).
t_s	Storage time.
t_{on}	Turn on time.
t_{off}	Turn off time.
t_r	Rise time.
t_f	Fall time.

The Circuit Designer's task is to design circuits and not, in general, to derive device application equations. He prefers to think of a transistor as a four-terminal black box which has known characteristics and to which certain application equations apply. Approximate equations are desirable because they are easier to remember and because they tend to reduce the required calculation time. However, the final answers will be approximate, and some degree of accuracy must be established.

One should not assume that any circuit solution for such parameters as A_v , A_i , R_{in} , R_o , etc. is exact in the rigid sense of the word regardless of the care taken with the solution. The

equivalent circuit, for example, is an approximation to the actual device. Also, the parameters of a particular transistor are not known exactly. Furthermore, these parameters vary as indicated later. The design task is not, however, hopeless because the designer is able to calculate appropriate parameters to sufficient accuracy. Calculated results for an amplifier are compared to measured results in Sec. 5-5.

Common Emitter

In the design of circuits, the usual black box (transistor) parameters of interest are voltage and current gains, and input and output impedances. An ac small-signal, T -equivalent circuit for the transistor in Fig. 5-5a is indicated in Fig. 5-5b.

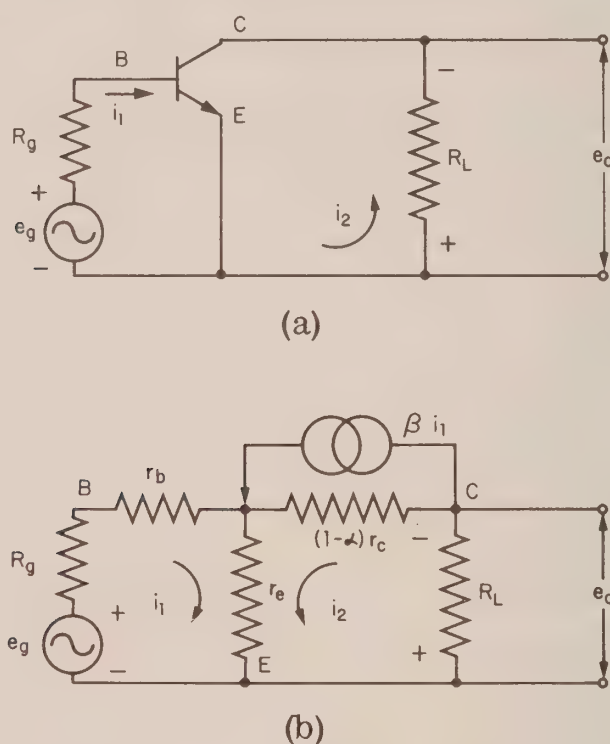


FIG. 5-5 Common-Emitter T -Equivalent Circuit

The parameters in Fig. 5-5 are defined in Table 5-1. Typical values for r_b , r_e , r_c , α , and β are as follows:

r_b	1 k Ω
r_e	25 Ω
r_c	1.5 M Ω
α	0.98
β	50

The first step in calculating the circuit parameters (A_i , A_v , R_{in} , R_o) is to write the two Kirchhoff loop equations.

$$\beta i_1 r_d = i_2 (r_e + r_d + R_L) + i_1 r_e$$

Solving for i_2 :

$$\begin{aligned} i_2 &= \frac{i_1 (\beta r_d - r_e)}{r_e + r_d + R_L} \\ &= \frac{i_1 (\alpha r_c - r_e)}{r_e + r_d + R_L} \end{aligned}$$

Writing the second loop equation:

$$\begin{aligned} e_g &= i_1 (R_g + r_b + r_e) + i_2 r_e \\ &= i_1 \left[R_g + r_b + r_e + \frac{r_e (\alpha r_c - r_e)}{r_e + r_d + R_L} \right] \end{aligned}$$

Solving for current gain from the first loop equation:

$$\begin{aligned} A_i &= \frac{-i_2}{i_1} \\ &= \frac{-(\alpha r_c - r_e)}{r_e + r_d + R_L} \end{aligned} \quad (5-8)$$

Since r_e is normally small, Eq. (5-8) can be simplified to Eq. (5-9)

$$A_i \cong \frac{-\alpha r_c}{r_d + R_L} \quad (5-9)$$

The input resistance is calculated as follows

$$\begin{aligned} R_{in} + R_g &= \frac{e_g}{i_1} \\ &= R_g + r_b + r_e + \frac{r_e (\alpha r_c - r_e)}{r_e + r_d + R_L} \\ R_{in} &= r_b + r_e \left(\frac{r_c + R_L}{r_e + r_d + R_L} \right) \text{ ohms} \end{aligned} \quad (5-10)$$

If r_d is much greater than $r_e + R_L$, the Eq. (5-10) can be simplified to Eq. (5-11)

$$R_{in} \cong r_b + (\beta + 1) r_e \text{ ohms} \quad (5-11)$$

Voltage gain is calculated as follows

$$\begin{aligned} e_o &= -i_2 R_L \\ &= \frac{-i_1 (\alpha r_c - r_e) R_L}{r_e + r_d + R_L} \\ A_V &= \frac{e_o}{e_g} \quad \text{where } e_g \text{ is as calculated from} \\ &\quad \text{the second loop equation.} \\ A_V &= \frac{-(\alpha r_c - r_e) R_L}{(r_e + r_d + R_L) (R_g + r_b + r_e) + r_e (\alpha r_c - r_e)} \quad (5-12) \end{aligned}$$

Note that Eq. (5-12) is still applicable if unbypassed resistance is added to the emitter and/or base lead. It is only necessary to replace r_e (or r_b) by the sum of r_e (or r_b) and the additional emitter (or base) resistance.

If R_g is much less than $r_b + r_e$ and r_c much greater than R_L and r_e , then Eq. (5-12) can be reduced to Eq. (5-13), which is somewhat easier to remember

$$A_v \cong \frac{-\beta R_L}{r_b + (\beta + 1) r_e} \quad (5-13)$$

If unbypassed resistance is added to the emitter lead, thereby introducing additional negative feedback, the quantity $(\beta + 1) R_e$ may become large, and Eq. (5-13) reduces to approximately $-R_L/R_e$.

Output resistance is equal to the open-circuit voltage divided by the short-circuit current, and the open-circuit voltage is equal to e_g multiplied by A_v where A_v is defined by Eq. (5-12) with R_L equal to ∞ . The generator voltage e_g is found from the second loop equation with R_L equal to zero

$$e_g = i_1 \left[R_g + r_b + r_e + \frac{r_e (\alpha r_c - r_e)}{r_e + r_d} \right]$$

The short-circuit current is equal to i_2 with R_L equal to zero

where i_2 is defined by the first loop equation

$$i_{sc} = \frac{i_1(\alpha r_c - r_e)}{r_e + r_d}$$

The output resistance is given, then, by Eq. (5-14)

$$\begin{aligned} R_o &= A_v \frac{e_g}{i_{sc}} \\ &= r_d + r_e \left(\frac{R_g + r_b + \alpha r_c}{R_g + r_b + r_e} \right) \text{ ohms} \end{aligned} \quad (5-14)$$

As R_g approaches ∞ , Eq. (5-14) reduces to approximately r_d .

The amplifier output resistance R'_o , for the case where R_L is not infinite, is given by Eq. (5-15) where R_o is defined by Eq. (5-14)

$$R'_o = \frac{R_o R_L}{R_o + R_L} \text{ ohms} \quad (5-15)$$

Power gain can be calculated by multiplying current gain by voltage gain.

Common Base

The common base stage is used less frequently than either the common-emitter or the common-collector (emitter-follower) stage. It is characterized by no phase inversion between the input and output signals, low input impedance, high output impedance, and current gain less than 1. The equivalent circuit for the common base amplifier is of the same configuration as Fig. 5-5 with r_b and r_e interchanged. The input current is then i_e , and the value of the current generator is αi_e . The resistance in parallel with the current generator is r_c rather than $(1 - \alpha)r_c$. Approximate equations relating to the common base connection are summarized at the end of this section.

Common Collector

The common collector connection is characterized by high input impedance, low output impedance, no phase inversion between input and output signals, and voltage gain of approximately 1. The small-signal equivalent circuit is indicated in Fig. 5-6.

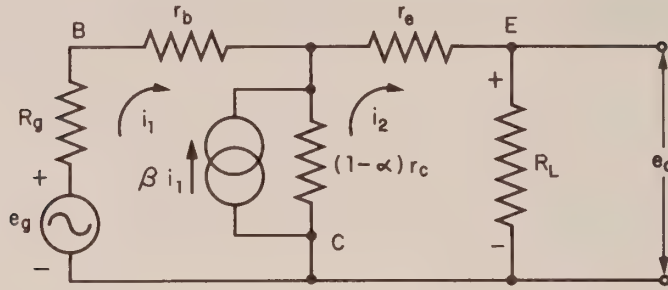


FIG. 5-6 Common-Collector T-Equivalent Circuit

The first step in solving for the circuit parameters (A_i , A_v , R_{in} , R_o) is to write the two Kirchhoff loop equations.

$$\beta i_1 r_d = i_2(r_e + r_d + R_L) - i_1 r_d$$

Solving for i_2 :

$$\begin{aligned} i_2 &= \frac{r_d(\beta + 1)i_1}{r_e + r_d + R_L} \\ &= \frac{r_c i_1}{r_e + r_d + R_L} \end{aligned}$$

Writing the second loop equation:

$$e_g = i_1(R_g + r_b) + i_2(r_e + R_L)$$

$$= i_1 \left[\frac{r_c(r_e + R_L)}{r_e + r_d + R_L} + R_g + r_b \right]$$

Current gain is found from the first loop equation:

$$\begin{aligned} A_i &= \frac{i_2}{i_1} \\ &= \frac{r_c}{r_e + r_d + R_L} \end{aligned} \tag{5-16}$$

If r_d is much greater than $r_e + R_L$, then Eq. (5-16) reduces to Eq. (5-17)

$$A_i \cong \beta + 1 \tag{5-17}$$

Input resistance is calculated as follows

$$\begin{aligned}
 R_{in} + R_g &= \frac{e_g}{i_1} \\
 &= \frac{r_c(r_e + R_L)}{r_e + r_d + R_L} + R_g + r_b \\
 R_{in} &= r_b + \frac{r_c(r_e + R_L)}{r_e + r_d + R_L} \text{ ohms}
 \end{aligned} \tag{5-18}$$

If r_d is much greater than $r_e + R_L$, then Eq. (5-18) can be reduced to Eq. (5-19)

$$\begin{aligned}
 R_{in} &\cong r_b + (\beta + 1)(r_e + R_L) \\
 &\cong r_b + (\beta + 1)R_L \text{ ohms}
 \end{aligned} \tag{5-19}$$

It is apparent from Eq. (5-19) that the input impedance of the common collector amplifier is a direct function of the load impedance. The significance is that the input circuit is not isolated from the output circuit to nearly the extent that it is with a vacuum tube cathode follower.

Voltage gain is equal to the output voltage divided by the generator voltage

$$\begin{aligned}
 e_o &= i_2 R_L \\
 &= \frac{i_1 r_c R_L}{r_e + r_d + R_L}
 \end{aligned}$$

The generator voltage is found from the second loop equation. Voltage gain is then given by Eq. (5-20)

$$\begin{aligned}
 A_v &= \frac{e_o}{e_g} \\
 &= \frac{r_c R_L}{r_c(r_e + R_L) + (r_b + R_g)(r_e + r_d + R_L)}
 \end{aligned} \tag{5-20}$$

If R_L approaches ∞ and r_c is much greater than $r_b + R_g$, then Eq. (5-20) reduces to Eq. (5-21)

$$A_v \cong \frac{r_c}{r_c + r_b + R_g} = 1 \quad (5-21)$$

Output resistance is equal to the open-circuit voltage divided by the short-circuit current. The open-circuit voltage is equal to the generator voltage multiplied by the voltage gain when R_L is equal to ∞ . The generator voltage is found from the second loop equation with R_L equal to zero.

$$e_g = i_1 \left(\frac{r_c r_e}{r_e + r_d} + R_g + r_b \right)$$

When R_L is equal to ∞ , the voltage gain is:

$$A_v = \frac{r_c}{r_c + r_b + R_g}$$

The short-circuit current is equal to i_2 when R_L is equal to 0

$$i_{sc} = \frac{r_c i_1}{r_e + r_d}$$

The output resistance is given by Eq. (5-22)

$$\begin{aligned} R_o &= \frac{A_v e_g}{i_{sc}} \\ &= r_e + \frac{r_d(r_b + R_g)}{R_g + r_b + r_c} \text{ ohms} \end{aligned} \quad (5-22)$$

If r_c is much greater than $R_g + r_b$, then Eq. (5-22) can be reduced to Eq. (5-23)

$$R_o \cong r_e + \frac{r_b + R_g}{\beta + 1} \text{ ohms} \quad (5-23)$$

Equation (5-23) indicates again that, in the emitter follower connection, the input and output circuits are not isolated.

Approximate T -equivalent circuit equations are summarized in Table 5-2, and one should know these equations from memory.

Table 5-2

	Common Base	Common Emitter	Common Collector
A_v	$\frac{\beta R_L}{r_b + \beta r_e}$	$\frac{-\beta R_L}{r_b + \beta r_e}$	1
A_i	α	$-\beta$	$\beta + 1$
R_o	r_c	r_d	$\frac{r_b + R_g}{\beta}$
R_{in}	$r_e + \frac{r_b}{\beta}$	$r_b + \beta r_e$	$r_b + \beta R_L$

Example 5-2

A buffer amplifier is to be designed for use in a control system to couple the control signal to a demodulator circuit. The control signal is sinusoidal with a frequency of 400 cps, and the generator impedance is 10 kΩ. The input circuit of the demodulator is comprised of a transformer, and the demodulator ac input impedance is 500 Ω.

The emitter follower connection is applicable because of its high input and low output impedances. Also, voltage amplification is not specified as a requirement. Although small-signal operation may not in actuality be the case, it is assumed for this example.

The selection of a transistor type would depend upon types used elsewhere in the system because of the desirability of minimizing the number of different types. For this example, a transistor is chosen with the following characteristics:

β	30	
r_e	33.5	Ω
r_b	500	Ω
r_c	1.67	MΩ

The proposed circuit configuration is indicated in Fig. 5-7, and the dc operating point is established for Class A operation. Selection of the dc load resistor R_L depends on the magnitude of the supply voltage E , the actual dynamic range required,

optimum operating current for the particular transistor type, etc. This problem is considered in other sections. For this example, R_L is specified as a $5.1\text{ K} \pm 5\%$, 1/4-W, composition resistor. Likewise, the other resistors are composition, 1/4-W, 5% types.

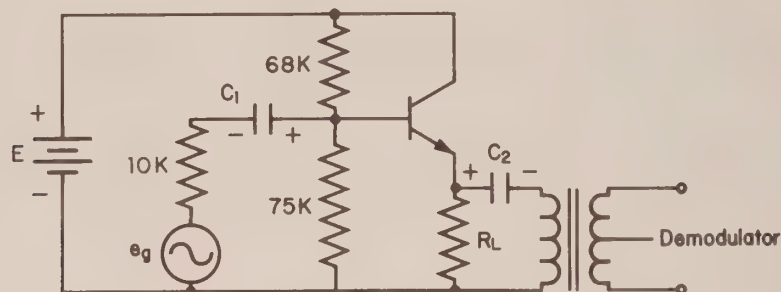


FIG. 5-7 Emitter-Follower Buffer Amplifier

The reactance of C_2 at 400 cps must be much less than $500\ \Omega$, the demodulator input impedance. A value for C_2 is calculated by arbitrarily setting X_C equal to $25\ \Omega$. The result is approximately $16\ \mu\text{F}$. A tantalum type capacitor is indicated, and a standard value of $22\ \mu\text{F} \pm 10\%$ with a voltage rating greater than $E/2$ is specified. The reactance of a $22\ \mu\text{F}$ capacitor at 400 cps is approximately $18\ \Omega$, which is considered negligible compared to the demodulator input impedance of $500\ \Omega$.

It is necessary to digress in order to examine RC coupling networks. Consider the circuit of Fig. 5-8. The low-frequency cutoff point is of interest. That is, the frequency at which the phase shift between input and output signals is 45° and the output amplitude is 70.7 percent of the mid-frequency value.

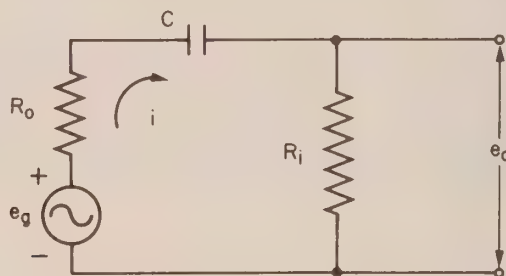


FIG. 5-8 RC Coupling Circuit

The mid-frequency gain is:

$$K_m = \frac{e_o}{e_g}$$

$$= \frac{R_i}{R_o + R_i}$$

where

$$X_C \approx 0$$

The low-frequency gain is found as follows:

$$\begin{aligned} K_1 &= \frac{e_o}{e_g} \\ &= \frac{i R_i}{e_g} \\ i &= \frac{e_g}{R_o + R_i - jX_C} \\ K_1 &= \frac{R_i}{R_o + R_i - jX_C} \end{aligned}$$

The ratio of K_1 to K_m is:

$$\frac{K_1}{K_m} = \frac{R_o + R_i}{R_o + R_i - jX_C}$$

At the low-frequency cutoff point, K_1/K_m is equal to $0.707 \angle 45^\circ$.

$$0.707 \angle 45^\circ = \frac{R_o + R_i}{R_o + R_i - jX_C}$$

For this equation to hold true, the magnitude of X_C must be equal to $R_o + R_i$

$$X_C = R_o + R_i$$

$$\frac{1}{2\pi f_1 C} = R_o + R_i$$

$$f_1 = \frac{1}{2\pi C (R_o + R_i)} \quad \text{cps} \quad (5-24)$$

Equation (5-24) indicates that the low-frequency cutoff point (f_1) is a function of the amplifier output impedance. Although

it was not stated that the demodulator was of the synchronous type, it is assumed to be such. In such a case, signal phase shift should be negligible, or the demodulator output characteristic will be adversely affected.

The object is to ensure that capacitors C_1 and C_2 introduce negligible signal phase shift. The next step is to calculate the amplifier output impedance.

The base biasing resistors are in parallel (ac-wise) with the generator resistance, and the equivalent input signal resistance is as follows:

$$R_s = \frac{10^3}{1/10 + 1/68 + 1/75}$$

$$= 8.5 \text{ K}\Omega$$

The output resistance is found from Eq. (5-23)

$$R_o = 33.5 + \frac{8500 + 500}{31}$$

$$\cong 424 \Omega$$

The output resistance of 424Ω is in parallel with the dc load resistance of $5.1 \text{ k}\Omega$. The complete output resistance R'_o is:

$$R'_o = \frac{(424)(5100)}{5524}$$

$$\cong 390 \Omega$$

The low-frequency cutoff point with the $22 \mu\text{F}$ coupling capacitor is now found from Eq. (5-24)

$$f_1 = \frac{10^6}{(2\pi)(22)(390 + 500)}$$

$$\cong 8 \text{ cps}$$

A cutoff frequency of 8 cps, compared to the signal frequency of 400 cps, is considered satisfactory, and the $22 \mu\text{F}$ capacitor value is retained.

Amplifier input resistance must be ascertained before the value of C_1 can be specified. The input resistance is found from Eq. (5-19) where R_L is equal to the dc load resistance in parallel

with the demodulator input impedance (and assuming that X_{C_2} is negligible).

$$R_{in} = 500 + (31)(33.5 + 455)$$

$$\cong 15.5 \text{ k}\Omega$$

The base biasing resistors are in parallel with the 15.5 K resistance. Hence, the amplifier input resistance R'_{in} is:

$$R'_{in} = \frac{10^3}{1/15.5 + 1/68 + 1/75}$$

$$\cong 10.8 \text{ k}\Omega$$

One can choose an input cutoff frequency equal to the output cutoff frequency of 8 cps. The value of capacitor C_1 can then be calculated from Eq. (5-24)

$$C_1 = \frac{10^{-3}}{16\pi(10 + 10.8)}$$

$$= 0.96 \mu\text{F}$$

A standard value of $1 \mu\text{F} \pm 10\%$ with a voltage rating greater than $E/2$ is specified for C_1 .

Voltage gain is the only other circuit parameter of interest, and this can be calculated from Eq. (5-20) after one decides what to do with the two base biasing resistors. These resistors are *not* in series with the transistor base resistance r_b ; they are instead in parallel with the transistor input impedance. The most direct method is to convert the bias resistors and the generator resistor into a Thévenin equivalent circuit. The parallel combination of 68 K and 75 K is approximately 35.6 k Ω . The Thévenin generator voltage is then

$$e_T = \frac{35.6 e_g}{35.6 + 10}$$

$$= 0.78 e_g$$

The Thévenin impedance is:

$$R_T = \frac{(35.6)(10)}{35.6 + 10}$$

$$= 7.8 \text{ k}\Omega$$

One can now use R_T in place of R_g in Eq. (5-20), and a load resistance R_L of 455 Ω . The result must be multiplied by 0.78 because of the bias resistor loading at the amplifier input

$$A_v = 0.78 \left[\frac{(1.67)(455)(10^6)}{(1.67)(488.5)(10^6) + (500 + 7.8K)(54K + 488.5)} \right]$$

$$\cong 0.47$$

An alternate method of calculating voltage gain is to use the amplifier input impedance number which was previously found (10.8 K). The attenuation from the voltage generator e_g to the base of the transistor is:

$$\frac{10.8}{10 + 10.8} = 0.52$$

Voltage gain is then found from Eq. (5-20) as before but with R_g equal to 0 and R_L equal to 455 Ω . The result is 0.9 which is then multiplied by 0.52 to give the previous answer of 0.47.

Obviously, a gain of 0.47 is considerably less than 1 but more than would be realized by connecting the signal generator with its output impedance to the demodulator directly. In such a case, the gain would be

$$K_g = \frac{500}{10,000 + 500}$$

$$= 0.0475$$

By using the emitter follower, there is an effective voltage gain over the direct connection of essentially 10.

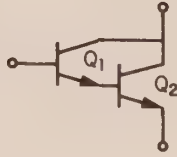
From the stated requirements, it is not known if a voltage gain of 0.47 is sufficient. It can be deduced from Eq. (5-20) that as β becomes very large the voltage gain approaches R_L divided by the sum of r_e and R_L .

$$A_v = \frac{455}{488.5}$$

$$= 0.93$$

Thus, the voltage gain would approach 0.93 if a transistor with a very large β and biasing resistors of higher magnitude were

used. The desired result can be effected by the following connections:



The two transistors (Q_1 and Q_2) can be considered as one transistor with a current gain of β_1 multiplied by β_2 and connected into the amplifier in place of the existing transistor. The stage gain would then approach 0.93 assuming that the parallel combination of the new biasing resistors to be much greater than the generator output impedance.

5-4 TRANSISTOR (HYBRID)

Transistor data sheets normally contain information in terms of hybrid parameters, and one must convert these parameters to equivalent T -parameters or derive equations to use them directly. Consideration of the hybrid equivalent circuit begins with a black-box representation for the transistor amplifier of Fig. 5-9.

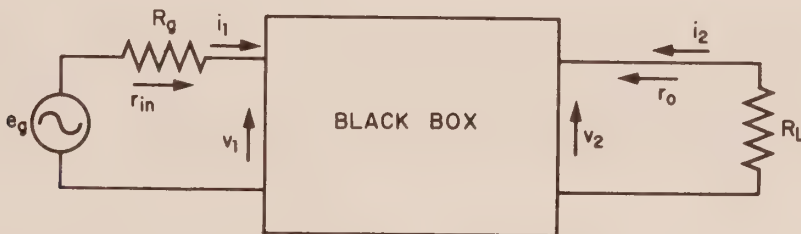


FIG. 5-9 Black Box Amplifier

Two equations describe the amplifier of Fig. 5-9, and these are as follows for the h -parameter case:

$$v_1 = i_1 h_{11} + v_2 h_{12} \quad (5-25)$$

$$i_2 = i_1 h_{21} + v_2 h_{22} \quad (5-26)$$

One can solve Eq. (5-25) for h_{11} in terms of v_1 and i_1 and Eq. (5-26) for h_{21} in terms of i_1 and i_2 if the output is ac short-circuited ($v_2 = 0$). The solutions are for the short-circuited case:

$$h_{11} = \frac{v_1}{i_1} \quad \text{input impedance}$$

$$h_{21} = \frac{i_2}{i_1} \quad \text{forward current gain}$$

Similarly, one can solve for h_{12} and h_{22} with the input ac open-circuited ($i_1 = 0$), and the solutions are:

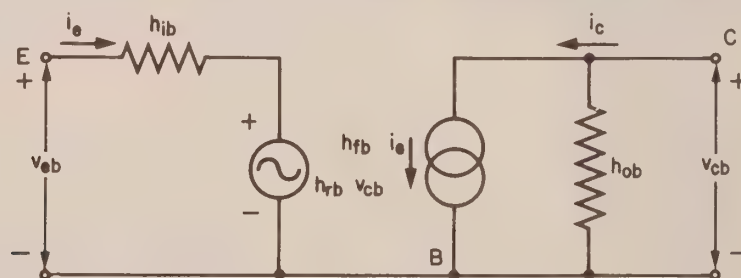
$$h_{12} = \frac{v_1}{v_2} \quad \text{reverse voltage transfer ratio}$$

$$h_{22} = \frac{i_2}{v_2} \quad \text{output admittance}$$

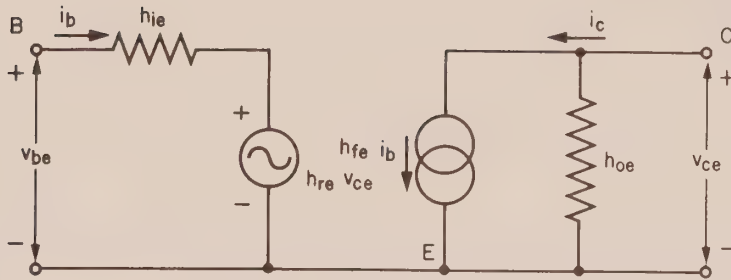
Thus, the h -parameters are defined specifically with the output ac short-circuited or the input ac open-circuited. Such has evolved because of the ease of parameter measurements, a factor which is particularly important to the device manufacturer.

The general subscripts associated with h_{11} , h_{12} , h_{21} , and h_{22} are usually changed to indicate the transistor configuration. That is, h_{ie} indicates common-emitter input impedance, h_{fe} common-emitter current gain, h_{re} common-emitter reverse voltage transfer ratio, and h_{oe} common-emitter output admittance. In the case of common base, the parameters are h_{ib} , h_{fb} , h_{rb} , and h_{ob} . Similarly, in the common-collector case, the parameters are h_{ic} , h_{fc} , h_{rc} , and h_{oc} .

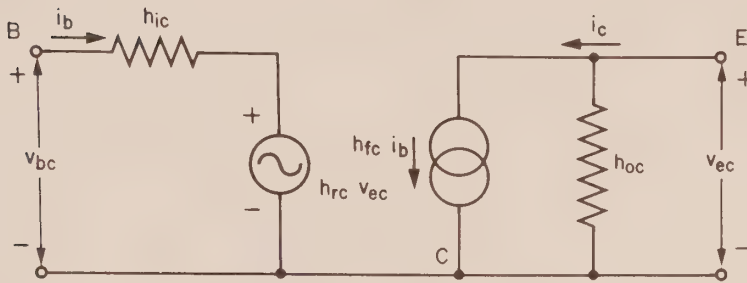
The h -parameter equivalent circuits for the transistor connected common base, common emitter, or common collector are indicated in Fig. 5-10a, b, and c, respectively.



(a) Common Base



(b) Common Emitter



(c) Common Collector

FIG. 5-10 Hybrid Equivalent Circuits

One could write equations to describe the circuits of Fig. 5-10, but it is more realistic to draw a new equivalent circuit which includes generator and load impedances and write equations to describe this circuit.

Common Emitter

An equivalent circuit for the common-emitter connected transistor is indicated in Fig. 5-11. Equations are then derived for R_{in} , R_o , A_i , and A_v .

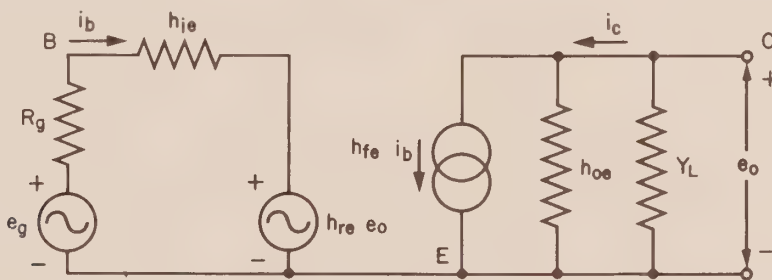


FIG. 5-11 Common-Emitter Equivalent Circuit

One first writes the two Kirchhoff loop equations

$$e_g = i_b(R_g + h_{ie}) + h_{re} e_o$$

$$e_o = -\frac{h_{fe} i_b}{h_{oe} + Y_L}$$

Solving for e_g

$$e_g = i_b \left(R_g + h_{ie} - \frac{h_{re} h_{fe}}{h_{oe} + Y_L} \right) \text{volts} \quad (5-27)$$

The input resistance plus the generator resistance is equal to e_g/i_b

$$\begin{aligned} R_{in} + R_g &= \frac{e_g}{i_b} \\ &= R_g + h_{ie} - \frac{h_{re} h_{fe}}{h_{oe} + Y_L} \\ R_{in} &= h_{ie} - \frac{h_{re} h_{fe}}{h_{oe} + Y_L} \text{ ohms} \end{aligned} \quad (5-28)$$

Voltage gain is equal to the output voltage divided by the input voltage

$$\begin{aligned} A_v &= \frac{e_o}{e_g} \\ A_v &= \frac{-h_{fe}}{(R_g + h_{ie})(h_{oe} + Y_L) - h_{re} h_{fe}} \end{aligned} \quad (5-29)$$

Current gain is found after solving for the current through Y_L

$$\begin{aligned} i_L &= \frac{Y_L i_c}{Y_L + h_{oe}} \\ i_c &= h_{fe} i_b \\ i_L &= \frac{h_{fe} Y_L i_b}{Y_L + h_{oe}} \\ A_i &= \frac{-i_L}{i_b} \\ &= \frac{-h_{fe} Y_L}{Y_L + h_{oe}} \end{aligned} \quad (5-30)$$

$$A_i = \frac{-h_{fe}}{1 + h_{oe} R_L} \quad (5-30)$$

(cont'd)

The output resistance is equal to the open-circuit voltage divided by the short-circuit current. The open-circuit voltage is equal to $A_v e_g$ where A_v is defined by Eq. (5-29) with Y_L equal to zero. The generator voltage e_g is found from Eq. (5-27) with Y_L equal to ∞

$$\begin{aligned} e_{op} &= A_v e_g \\ &= \frac{-i_b h_{fe} (R_g + h_{ie})}{h_{oe} (R_g + h_{ie}) - h_{re} h_{fe}} \end{aligned}$$

$$i_{sc} = -h_{fe} i_b$$

$$R_o = \frac{1}{h_{oe} - h_{re} h_{fe} / (R_g + h_{ie})} \quad \text{ohms} \quad (5-31)$$

The common-base and common-collector equations are similar to the common-emitter equations. However, the actual direction of the current i_c is opposite to that shown in Fig. 5-10a and c, and the result is that h_{fb} and h_{fc} are negative quantities.

Common Base

$$R_{in} = h_{ib} + \frac{h_{rb} |h_{fb}|}{h_{ob} + Y_L} \quad (5-32)$$

$$A_v = \frac{|h_{fb}|}{(R_g + h_{ib})(h_{ob} + Y_L) + h_{rb} |h_{fb}|} \quad (5-33)$$

$$A_i = \frac{|h_{fb}|}{1 + h_{ob} R_L} \quad (5-34)$$

$$R_o = \frac{1}{h_{ob} + h_{rb} |h_{fb}| / (R_g + h_{ib})} \quad (5-35)$$

Common Collector

$$R_{in} = h_{ic} + \frac{h_{rc} |h_{fc}|}{h_{oc} + Y_L}$$

(5-36)

$$A_v = \frac{|h_{fc}|}{(R_g + h_{ic})(h_{oc} + Y_L) + h_{rc} |h_{fc}|}$$

(5-37)

$$A_i = \frac{|h_{fc}|}{1 + h_{oc} R_L}$$

(5-38)

$$R_o = \frac{1}{h_{oc} + h_{rc} |h_{fc}| / (R_g + h_{ic})}$$

(5-39)

Transistor specification sheets usually define such parameters as h_{FE} , h_{fe} , h_{ib} , h_{rb} , and h_{ob} . Conversion from one set of parameters to another is often necessary, and Table 5-3 lists the more useful approximate conversions.

Table 5-3 Parameter Conversions

	Common Base	Common Emitter	Common Collector	Approximate T-Equivalent
α	$ h_{fb} $	$\frac{h_{fe}}{1 + h_{fe}}$	$\frac{ h_{fc} - 1}{ h_{fc} }$	$\frac{\beta}{\beta + 1}$
r_e	$h_{ib} - \frac{h_{rb}(1 - h_{fb})}{h_{ob}}$	$\frac{h_{re}}{h_{oe}}$	$\frac{1 - h_{rc}}{h_{oc}}$	
r_b	$\frac{h_{rb}}{h_{ob}}$	$h_{ie} - \frac{h_{re}(1 + h_{fe})}{h_{oe}}$	$h_{ic} - \frac{ h_{fc} (1 - h_{rc})}{h_{oc}}$	
r_c	$\frac{1 - h_{rb}}{h_{ob}}$	$\frac{1 + h_{fe}}{h_{oe}}$	$\frac{ h_{fc} }{h_{oc}}$	
h_{fe}	$\frac{ h_{fb} }{1 - h_{fb} }$		$ h_{fc} - 1$	β
h_{ie}	$\frac{h_{ib}}{1 - h_{fb} }$		h_{ic}	$r_b + (\beta + 1)r_e$

Table 5-3 Parameter Conversion (Con't.)

	Common Base	Common Emitter	Common Collector	Approximate T-Equivalent
h_{re}	$\frac{h_{ib} h_{ob}}{1 - h_{fb} } - h_{rb}$		$1 - h_{rc}$	$\frac{r_e(\beta + 1)}{r_c}$
h_{oe}	$\frac{h_{ob}}{1 - h_{fb} }$		h_{oc}	$\frac{1}{r_d}$
$ h_{fb} $		$\frac{h_{fe}}{1 + h_{fe}}$	$\frac{ h_{fc} - 1}{ h_{fc} }$	α
h_{ib}		$\frac{h_{ie}}{1 + h_{fe}}$	$\frac{h_{ic}}{ h_{fc} }$	$r_e + \frac{r_b}{\beta + 1}$
h_{rb}		$\frac{h_{ie} h_{oe}}{1 + h_{fe}} - h_{re}$	$(h_{rc} - 1) + \frac{h_{ic} h_{oc}}{ h_{fc} }$	$\frac{r_b}{r_c}$
h_{ob}		$\frac{h_{oe}}{1 + h_{fe}}$	$\frac{h_{oc}}{ h_{fc} }$	$\frac{1}{r_c}$

The approximate r -parameter equations which were previously derived for the common emitter amplifier can be related to the h -parameters. For instance, Eq. (5-11) (input resistance) is equal to h_{ie} . If an unbypassed resistance R_E is added in series with the emitter lead, the amplifier input resistance would be equal to $h_{ie} + (\beta + 1)R_E$ which is equal to $h_{ie} + (h_{fe} + 1)R_E$. Similarly, if a resistance R_B is added in series with the base lead, the input resistance would be equal to $h_{ie} + R_B$. Equation (5-40) is an approximate equation for (common-emitter) amplifier input resistance where external resistors are added:

$$R_{in} = h_{ie} + R_B + (h_{fe} + 1)R_E \text{ ohms} \quad (5-40)$$

Equation (5-13) (voltage gain) can also be expressed in terms of h -parameters, and this is illustrated by Eq. (5-41) where R_{in} is defined by Eq. (5-40)

$$A_v = - \frac{h_{fe} R_L}{R_{in}} \quad (5-41)$$

Equation (5-14) (output resistance) can be approximated to r_d which is equal to $1/h_{oe}$. Thus, output resistance is approximately equal to $1/h_{oe}$.

One can also convert Eq. (5-9) (current gain) to an h -parameter equivalent. This is illustrated by Eq. (5-42)

$$A_i = -\frac{|h_{fb}|}{(1/h_{oe} + R_L)(h_{ob})} \quad (5-42)$$

5.5 TRANSISTOR AMPLIFIER PARAMETERS

One must ultimately apply design equations to actual problems. It is the purpose of this section to compare calculated and experimental results for a common-emitter amplifier. The previously derived approximate equations are used to establish the accuracy of these equations. A problem usually exists in that the particular parameters of a given transistor are not known accurately, and calculated results may differ appreciably from experimental results for this reason unless a method of gain stabilization is employed. However, an unstabilized-voltage amplifier is depicted in Fig. 5-12, and the transistor parameters are defined as follows:

$$\alpha = 0.937$$

$$r_e = 33.5 \quad \Omega$$

$$r_b = 750 \quad \Omega$$

$$r_c = 1.67 \text{ M}\Omega$$

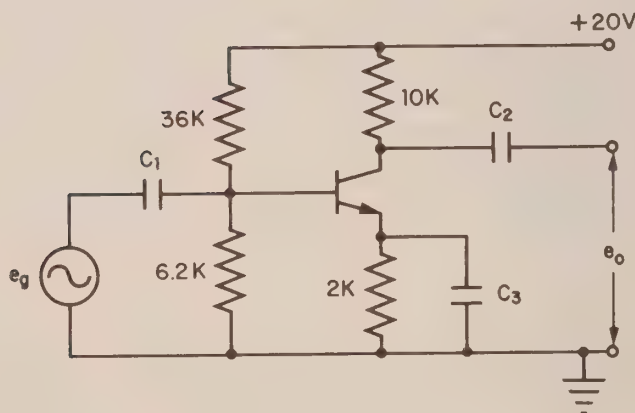


FIG. 5-12 Voltage Amplifier

The capacitive reactances of C_1 , C_2 , and C_3 are negligible at the signal frequency. Input resistance, voltage gain, and

output resistance are found from the equations in Table 5-2.

$$\begin{aligned} R_{in} &\cong r_b + \beta r_e \\ &= 750 + (15)(33.5) \\ &= 1,250 \Omega \end{aligned}$$

The actual amplifier input resistance R'_{in} is equal to the parallel combination of R_{in} and the two base-biasing resistors

$$\begin{aligned} R'_{in} &= \frac{10^3}{1/1.25 + 1/6.2 + 1/36} \\ &= 1.0 \text{ k}\Omega \quad (1.2\text{K experimental}) \end{aligned}$$

Voltage gain is found as follows:

$$\begin{aligned} A_v &\cong \frac{-\beta R_L}{r_b + \beta r_e} \\ &= -\frac{(15)(10\text{K})}{1,250} \\ &= -120 \quad (-112 \text{ experimental}) \end{aligned}$$

The output resistance is approximately equal to r_d in parallel with the 10 K load resistance.

$$\begin{aligned} R_o &\cong \frac{r_d R_L}{r_d + R_L} \\ &= \frac{(105)(10\text{K})}{115} \\ &= 9.15 \text{ k}\Omega \quad (9.1\text{K experimental}) \end{aligned}$$

Ordinarily one would not expect better than 5 percent correlation between calculated and experimental results. Resistor tolerances are usually ± 5 percent (depending upon what one specifies), and transistor parameters are not known exactly.

If one calculates voltage gain from the more elaborate equation. (Eq. 5-12), the result is -110 , which agrees quite well with the measured value of -112 .

It should be noted, however, that one seldom designs a single-stage amplifier with a voltage gain of 100 or more. Ten to twenty is a typical range of amplification for a single-stage amplifier. A reduction in gain can be accomplished by including unbypassed resistance in series with the emitter lead, thereby incorporating gain stabilization as well. For instance, the voltage gain reduces to approximately -5 , $(-10/2)$, if capacitor C_3 is disconnected. To find the gain more accurately, one can solve Eq. (5-13)

$$\begin{aligned} A_v &= - \frac{\beta R_L}{r_b + (\beta + 1) r_e} \\ &= - \frac{(15)(10K)}{750 + (16)(33.5 + 2K)} \\ &= -4.5 \text{ (From Eq. 5-13)} \end{aligned}$$

If one solves the complete voltage-gain equation (Eq. 5-12), the answer is -4.45 .

$$A_v = -4.45 \text{ (From Eq. 5-12)}$$

The results from Eqs. (5-12) and (5-13) agree to within approximately one percent. The factor worth noting is that the approximate equations yield better results where gain stabilization is employed than they do for unstabilized configurations.

5-6 DESIGN EXAMPLE

An amplifier is to be designed to amplify by a factor of 5 ± 10 percent a 1,000-cps sinusoidal tone signal. Small signal, room temperature operation can be assumed. The supply voltage is +20 vdc. The source impedance is $5 \text{ k}\Omega$, and the ac load impedance is $3 \text{ k}\Omega$. Voltage amplification of 5 ± 10 percent is to be obtained from production units. That is, component tolerances must be considered in the design.

For maximum power transfer, the amplifier input impedance should be equal to the source impedance ($5 \text{ k}\Omega$), and the output impedance should be equal to the ac load impedance ($3 \text{ k}\Omega$). These conditions are not requirements, but they serve as a starting point for the design.

It would appear that a single-stage amplifier is appropriate if a high gain transistor is specified. Accordingly, a transistor

type number is selected with the following characteristics:

Current Transfer Ratio (h_{fe})	Min	Max
($I_c = 1 \text{ mA}$, $V_{ce} = 5 \text{ V}$)	50	200
($I_c = 5 \text{ mA}$, $V_{ce} = 10 \text{ V}$)	70	300

Input Resistance (h_{ib})		
($I_c = 1 \text{ mA}$, $V_{cb} = 5 \text{ V}$)	24	34
($I_c = 5 \text{ mA}$, $V_{cb} = 10 \text{ V}$)	4	8
($I_c = 3 \text{ mA}$, $V_{cb} = 10 \text{ V}$)	6	12

Voltage Feedback Ratio (h_{rb})		
($I_c = 1 \text{ mA}$, $V_{cb} = 5 \text{ V}$)		5×10^{-4}
($I_c = 5 \text{ mA}$, $V_{cb} = 10 \text{ V}$)		5×10^{-4}

Output Conductance (h_{ob})		
($I_c = 1 \text{ mA}$, $V_{cb} = 5 \text{ V}$)	0.1	$0.5 \mu \text{ mho}$
($I_c = 5 \text{ mA}$, $V_{cb} = 10 \text{ V}$)	0.1	$1.0 \mu \text{ mho}$

A dc operating point of V_{ce} equal to 10 V and I_c equal to 3 mA is selected because the transistor parameters are optimized in this region and because Class A operation suggests a value of V_{ce} which is equal to one-half of the supply voltage. Operating point selection and stabilization are discussed more fully in Chap. 7. The proposed stage is depicted in Fig. 5-13.

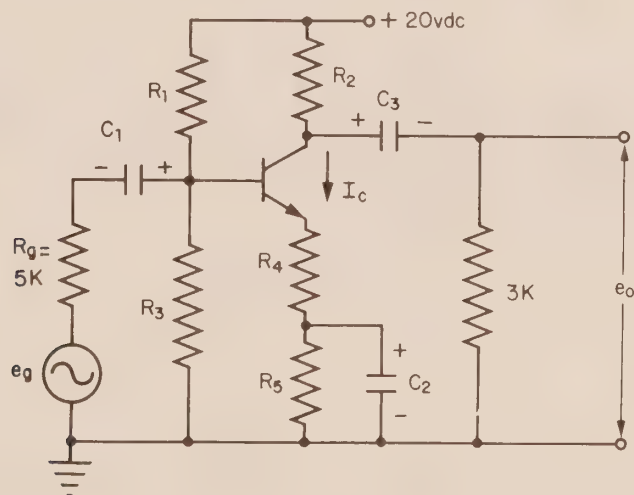


FIG. 5-13 Gain-Stabilized Amplifier

If a voltage drop of 10 V is to exist from collector to emitter at a collector current of 3 mA, then the sum of R_2 , R_4 , and R_5 must be equal to 3.3 k Ω . For reasons of operating point stabilization, the sum of R_4 and R_5 is chosen to be approximately 600 Ω which means that R_2 must be 2.7 k Ω . It is recognized that exact Class A operation will not be realized, but the amplifier dynamic range is considered adequate for this problem. (The collector dc operating point is: $20 - (2.7)(3) = 12$ V.) The magnitudes of the known resistors are specified

$$R_2 = 2.7 \text{ k}\Omega$$

$$R_4 + R_5 = 600 \text{ }\Omega$$

Resistor values for R_1 and R_3 are calculated from operating point considerations to be as follows

$$R_1 = 120 \text{ k}\Omega$$

$$R_3 = 20 \text{ k}\Omega$$

The magnitudes of resistors R_1 and R_3 should be as large as is practicable to minimize loading of the input signal. Thévenin's Theorem is used to reduce the input resistor network (R_1 , R_3 , and R_g) and the signal generator e_g into an equivalent voltage generator with the proper Thévenin output impedance.

The parallel combination of resistors R_1 and R_3 is equal to approximately 17 k Ω . The gain reduction factor as a result of input resistors R_1 and R_3 is as follows:

$$K = \frac{17}{17 + 5}$$

$$= 0.77$$

Therefore, an amplification of 6.5, $(5/0.77)$, rather than 5, is required from the amplifier.

The Thévenin output impedance is equal to the parallel combination of R_g and 17 k Ω

$$R_T = \frac{(5)(17)}{22}$$

$$= 3.86 \text{ k}\Omega$$

An ac equivalent to the circuit of Fig. 5-13 is illustrated in Fig. 5-14.

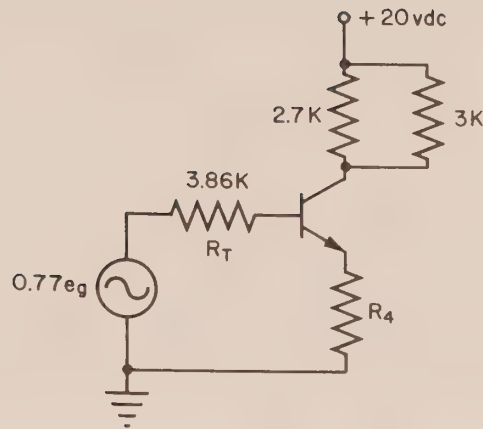


FIG. 5-14 AC Equivalent Circuit

The equivalent ac load impedance (R_{ac}) is equal to the parallel combination of the 2.7 K resistor and the 3 K resistor or 1.42 k Ω .

One can now use approximate Eqs. (5-40) and (5-41) to complete the initial design. As indicated in Sec. 5-5, these equations are sufficiently accurate for a problem of the present type. Equations (5-40) and (5-41) are rewritten here in a form applicable to this problem:

$$R_{in} = h_{ie} + (h_{fe} + 1) R_4 \quad (5-40)$$

$$A_v = - \frac{(h_{fe})(1.42K)}{R_{in}} \quad (5-41)$$

Nominal transistor parameters are assumed during the design phase as follows:

$$h_{fe} = 100 \text{ nominal}$$

$$h_{ib} = 9 \text{ } \Omega \text{ nominal}$$

Table 5-3 is used to find h_{ie} in terms of h_{ib} and h_{fb} in terms of h_{fe}

$$h_{ie} = \frac{h_{ib}}{1 - |h_{fb}|}$$

$$h_{fb} = \frac{h_{fe}}{1 + h_{fe}}$$

Solving for h_{ie} :

$$\begin{aligned} h_{ie} &= \frac{9}{1 - 100/101} \\ &= 909 \quad \Omega \end{aligned}$$

Voltage gain, as expressed by Eq. (5-41), is the ratio of the transistor ac output voltage to the transistor ac input voltage, and the input voltage is not equal to the generator voltage ($0.77 e_g$) in Fig. 5-14 unless the generator output impedance is zero (rather than $3.86 \text{ k}\Omega$). Equation (5-43) expresses voltage gain where the Thévenin generator output impedance R_T is included (see Fig. 5-14).

$$\begin{aligned} A_v &= - \left[\frac{(h_{fe})(R_L)}{R_{in}} \right] \left[\frac{R_{in}}{R_{in} + R_T} \right] \\ A_v &= - \frac{(h_{fe})(R_L)}{R_{in} + R_T} \end{aligned} \quad (5-43)$$

As the load resistance R_L increases in magnitude, Eq. (5-43) becomes more inaccurate because of the shunting effect of the transistor output admittance h_{oe} . Thus, Eq. (5-44) is more applicable for larger values of R_L (say, those greater than $2 \text{ k}\Omega$) if better accuracy is required

$$A_v = - \frac{h_{fe}}{(R_{in} + R_T)(Y_L + h_{oe})} \quad (5-44)$$

The required input resistance for a voltage gain of 6.5 is calculated from Eq. (5-43)

$$6.5 = \frac{(100)(1,420)}{R_{in} + 3,860}$$

$$R_{in} = 18 \text{ k}\Omega$$

A value for R_4 is calculated from Eq. (5-40)

$$18 \text{ K} = 909 + (101)(R_4)$$

$$R_4 = 170 \quad \Omega$$

It was previously established that the sum of R_4 and R_5 should be $600\ \Omega$. Therefore, the value of R_5 is $430\ \Omega$. The design values are summarized as follows:

$$R_1 = 120\ \text{k}\Omega$$

$$R_2 = 2.7\ \text{k}\Omega$$

$$R_3 = 20\ \text{k}\Omega$$

$$R_4 = 170\ \Omega$$

$$R_5 = 430\ \Omega$$

A worst-case analysis is necessary to determine the percentage variation in voltage gain as a function of transistor parameter variations. As indicated by graphs supplied by the manufacturer, the limitation on h_{fe} at an emitter current of 3 mA is 50 to 250 and on h_{ib} , 6 to 12. Worst case for the amplifier is a combination of 250 and 6 or 50 and 12, but such a combination is unlikely to occur because of inherent transistor characteristics. Thus, voltage gain is calculated first with h_{fe} equal to 250 and h_{ib} equal to 12, and then it is calculated with h_{fe} equal to 50 and h_{ib} equal to 6. Gain calculation for the case where:

$$h_{fe} = 250$$

$$h_{ib} = 12$$

$$h_{ie} = (h_{fe} + 1)(h_{ib})$$

$$= 3.01\ \text{k}\Omega$$

Calculating R_{in} from Eq. (5-40)

$$R_{in} = 3.01\text{K} + (251)(170)$$

$$= 45.7\ \text{k}\Omega$$

Calculating A_v from Eq. (5-43):

$$A_v = - \frac{(250)(1.42\text{K})}{47.6\text{K} + 3.86\text{K}}$$

$$= -7.14$$

The percentage variation in voltage gain is

$$\begin{aligned}\% \text{ variation} &= \frac{(100)(7.14 - 6.5)}{6.5} \\ &= 10.5\end{aligned}$$

Voltage gain is next calculated for the case where h_{fe} is equal to 50 and h_{ib} is equal to 6 ($h_{ie} = 306 \Omega$). Calculating R_{in} from Eq. (5-40):

$$\begin{aligned}R_{in} &= 306 + (51)(170) \\ &= 8.98 \text{ k}\Omega\end{aligned}$$

Calculating A_v from Eq. (5-43):

$$\begin{aligned}A_v &= -\frac{(50)(1.42 \text{ K})}{8.98 \text{ K} + 3.86 \text{ K}} \\ &= -5.5\end{aligned}$$

The percentage variation in voltage gain is:

$$\begin{aligned}\% \text{ variation} &= \frac{(100)(5.5 - 6.5)}{6.5} \\ &= -15.4\end{aligned}$$

The variation in one case is 10.5 percent and in the other case -15.4 percent for a total variation of approximately 26 percent. If ± 1 percent resistors are specified for resistors R_2 and R_4 , and it is assumed that the 3 K ac load impedance is nonvariable, then a total percentage gain variation of approximately 27.5 can be predicted on a worst-case basis. This, of course, exceeds the allowable gain tolerance of ± 10 percent.

Several corrective possibilities exist. Resistor R_4 can be specified as selectable for each amplifier to ensure the proper voltage gain, or a potentiometer can be specified rather than a fixed resistor. Amplifier production costs would tend to increase for either choice, however. Another alternative is to limit the allowable range in h_{fe} . The transistor manufacturer will accept such orders at an increase in unit price. Of course, a two-stage amplifier could be designed with additional negative feedback to stabilize voltage gain, but such a solution would result in an expensive amplifier. An attractive possibility from the designer's standpoint is to change the specification from ± 10 percent to say ± 15 percent on a worst-case basis. Specifications are frequently modified to agree with actual unit performance, and it is assumed that this solution is practical in the present design.

A modification to the design is still necessary because the variation at h_{fe} equal to 50 exceeds 15 percent in magnitude. A new nominal value for R_4 must be calculated. At h_{fe} equal to 50 and h_{ib} equal to 6, a gain variation of -13.5 percent is allowable. The gain under such conditions is calculated as follows:

$$-13.5 = \frac{(100)(A - 6.5)}{6.5}$$

$$|A| = 5.62$$

Calculating R_{in} from Eq. (5-43):

$$-5.62 = - \frac{(50)(1.42K)}{R_{in} + 3.86K}$$

$$R_{in} = 8.74 \text{ k}\Omega$$

Calculating R_4 from Eq. (5-40):

$$8.74K = 306 + 51 R_4$$

$$R_4 = 168 \text{ }\Omega$$

The voltage gain is recomputed at h_{fe} equal to 250 and h_{ib} equal to 12 to be -7.35 which results in a gain variation of 13.1 percent.

Values for the coupling and bypass capacitors in Fig. 5-13 can be found from Eq. (5-24) if a cutoff frequency f_1 is assumed. Alternately, one can assume that the capacitive reactance at the signal frequency should be 0.01 times the associated resistance. For instance, let X_{C1} be equal to 38Ω in magnitude, X_{C2} equal to 4.3Ω , and X_{C3} equal to 14Ω . Capacitor values are then calculated at a frequency of 1,000 cps to be as follows:

$$C_1 = 4.2 \text{ }\mu\text{F}$$

$$C_2 = 37 \text{ }\mu\text{F}$$

$$C_3 = 11.4 \text{ }\mu\text{F}$$

Polarized tantalum-type capacitors are specified for size reasons

$$C_1 = 4.7 \text{ }\mu\text{F} \pm 10\%, 15 \text{ vdc}$$

$$C_2 = 47 \text{ }\mu\text{F} \pm 10\%, 15 \text{ vdc}$$

$$C_3 = 15 \text{ }\mu\text{F} \pm 10\%, 20 \text{ vdc}$$

The resistors are specified as follows where the values for R_2 and R_4 are the nearest one percent standard values:

$$R_1 = 120 K \pm 5\%, \frac{1}{4} W, \text{ carbon composition}$$

$$R_2 = 2.74 K \pm 1\%, \frac{1}{4} W, \text{ metal film}$$

$$R_3 = 20 K \pm 5\%, \frac{1}{4} W, \text{ carbon composition}$$

$$R_4 = 169 \pm 1\%, \frac{1}{4} W, \text{ metal film}$$

$$R_5 = 430 \pm 5\%, \frac{1}{4} W, \text{ carbon composition}$$

In actual practice, the circuit should be constructed and thoroughly tested in the laboratory before the design would be released to production. *Experimental* results were as follows for the specified circuit

$$h_{fe} = 145$$

$$V_{CE} = 9.87 \text{ vdc}$$

$$V_C = 11.7 \text{ vdc}$$

$$A = -5.40$$

If one calculates voltage gain for the case of h_{fe} equal to 145 and h_{ib} equal to 9, using Eqs. (5-40) and (5-43), the result is -5.42 which correlates to the measured value to within approximately 1.5 percent.

PROBLEMS

- 5-1 A vacuum-tube amplifier is depicted in Fig. 1, and the tube characteristics are defined as follows:

$$r_p = 10 \text{ k}\Omega$$

$$\mu = 30$$

Small-signal, mid-frequency operation is specified, and the capacitive reactances of C_1 , C_2 , and C_3 are negligible at the frequencies of interest.

- What is the voltage gain e_o/e_g ?
- What is the amplifier output impedance?
- If capacitor C_2 is disconnected, what is the voltage gain?

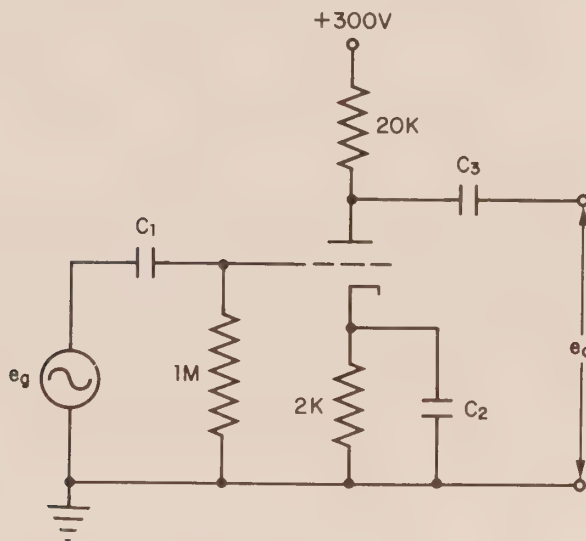


FIG. 1 Voltage Amplifier

- 5-2 A common-emitter amplifier is depicted in Fig. 2, and the transistor characteristics are defined as follows:

$$h_{fe} = 100$$

$$h_{ib} = 30 \Omega$$

$$h_{rb} = 4 \times 10^{-4}$$

$$h_{ob} = 0.3 \mu \text{ mhos}$$

Small-signal, mid-frequency operation is specified, and the capacitive reactances of C_1 and C_2 are negligible at the frequencies of interest.

- What is the amplifier input impedance if R_L is equal to ∞ ?
- If R_g is equal to zero and R_L is equal to ∞ , what is the voltage gain e_o/e_g ?
- If R_g is equal to $1\text{ k}\Omega$ and R_L is equal to $10\text{ k}\Omega$, what is the voltage gain e_o/e_g ?
- With the conditions of part *c* and a desired amplifier low-frequency (f_1) cutoff point of 100 cps , specify values for coupling capacitors C_1 and C_2 .

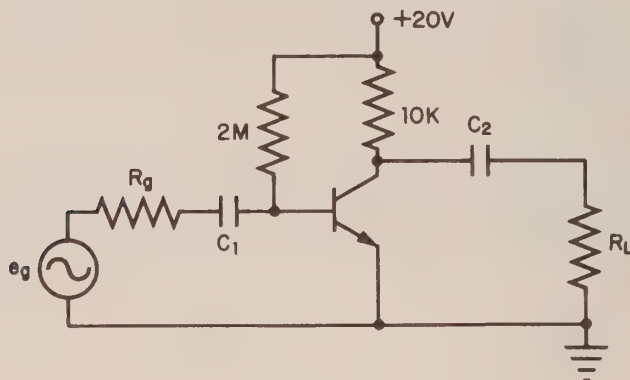


FIG. 2 Common-Emitter Amplifier

- 5-3 The amplifier of Fig. 3 was designed to drive a capacitive load. Small-signal, sinusoidal operation is assumed, and the capacitive reactances of the coupling and bypass capacitors are negligible at all frequencies of interest. The transistor characteristics are specified as follows:

$$h_{fe} = 100$$

$$h_{ie} = 1\text{ k}\Omega$$

$$h_{re} = 3.5 \times 10^{-4}$$

$$h_{oe} = 50 \times 10^{-6}\text{ mhos}$$

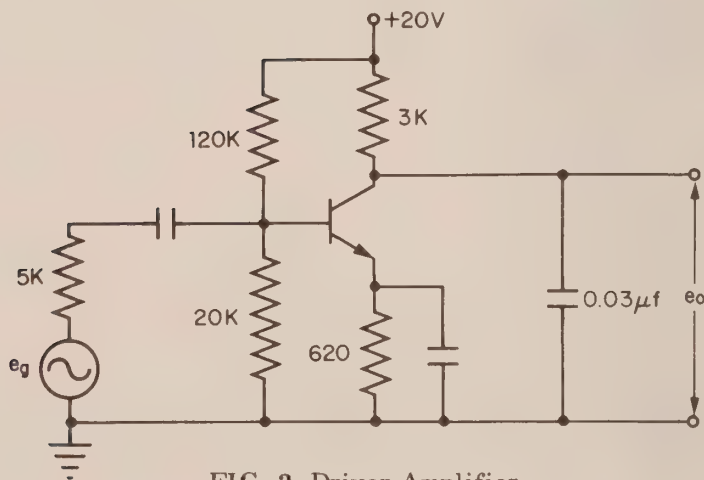


FIG. 3 Driver Amplifier

- a. What is the amplifier output impedance with the $0.03\ \mu\text{F}$ capacitor disconnected?
- b. What is the upper 3-dB frequency with the capacitor connected as shown in Fig. 3? That is, at what frequency is the magnitude of the voltage gain e_o/e_g equal to 0.707 of the low-frequency voltage gain?

5-4 The amplifier of problem 5-3 was redesigned, using the same transistor, to drive the same load. The common collector connection was used as indicated in Fig. 4. What is the upper 3-dB frequency in this case?

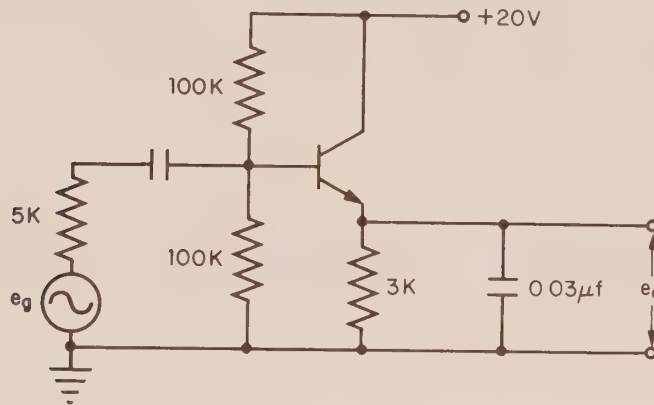


FIG. 4 Emitter-Follower Driver

5-5 The voltage gain of the amplifier which is depicted in Fig. 5 is frequency-dependent. Write an approximate expression, similar to Eq. (5-43), for the voltage gain e_o/e_g . Assume linear, sinusoidal operation.

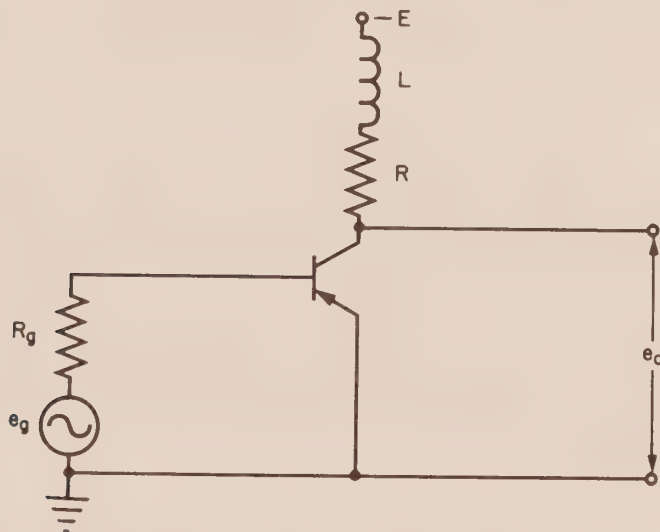


FIG. 5 Frequency-Dependent Amplifier

- 5-6 Considerable input capacitance is associated with the amplifier of Fig. 6. The transistor parameters are specified as follows:

$$h_{fe} = 100$$

$$h_{ie} = 1 \text{ k}\Omega$$

$$h_{re} = 3.5 \times 10^{-4}$$

$$h_{oe} = 50 \times 10^{-6}$$

The signal-generator voltage is defined by the following equation:

$$e_g = 0.1 \sin(2513t) \text{ volts}$$

Assume that the capacitive reactances of the coupling and bypass capacitors are negligible at the frequency of interest.

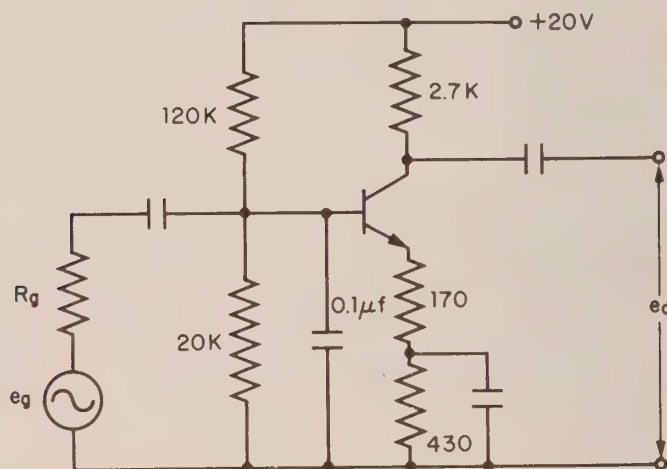


FIG. 6 Voltage Amplifier

- What is the voltage gain e_o/e_g if R_g is equal to zero, and what is the peak value of the output signal?
 - What is the voltage gain e_o/e_g if R_g is equal to $5 \text{ k}\Omega$?
- 5-7 A four-terminal black box has an output vs. input characteristic of -3 , ($e_o/e_{in} = -3$), where the input voltage is defined by the following equation

$$e_{in} = 2 \sin(2513t) \text{ volts}$$

Replace the black box with a device which has the same output-vs.-input characteristic.

5-8 In a two-phase, 400-cps system, two sinusoidal signals are required with a phase relationship of 90° . The design of the circuit depicted in Fig. 7 is to be completed to satisfy the following requirement

$$e_o/e_g = 5 \angle 90^\circ$$

Both transistors are of the same type with the following characteristics

$$h_{fe} = 100$$

$$h_{ie} = 3.03 \text{ k}\Omega$$

$$h_{re} = 5.1 \times 10^{-4}$$

$$h_{oe} = 30.3 \times 10^{-6} \text{ mhos}$$

Complete the design assuming nominal component values. Specify the potentiometer resistance rating, and indicate the nominal setting. For various reasons, the minimum permissible value for R_1 is $1 \text{ k}\Omega$. The voltage e_g is defined by the following equation

$$e_g = 0.5 \sin(2513 t) \text{ volts}$$

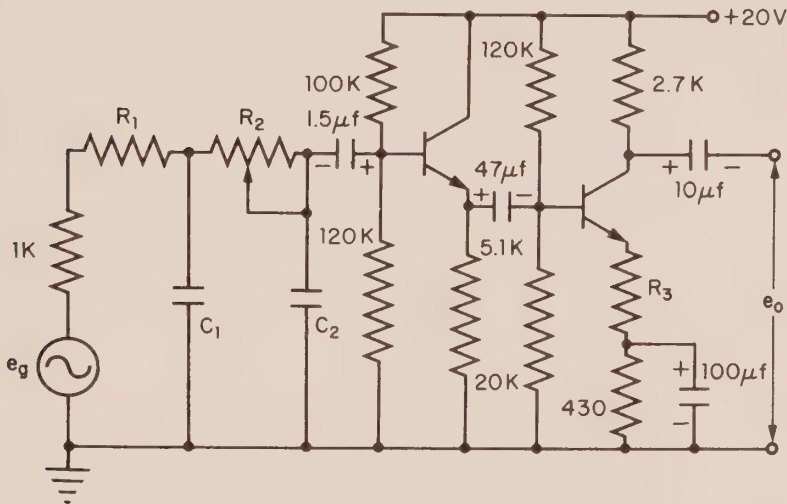


FIG. 7 Design Problem

BIBLIOGRAPHY

GE Staff: "GE Transistor Manual," 7th ed., chap. 2, General Electric, 1964.

- Hunter: "Handbook of Semiconductor Electronics," chap. 11,
McGraw-Hill Book Company, New York, 1956.
- Millman and Taub: "Pulse and Digital Circuits," chap. 18,
McGraw-Hill Book Company, New York, 1956.
- Landee, Davis, and Albrecht: "Electronic Designers' Hand-
book, pp. 2-57 to 2-82, McGraw-Hill Book Company, New
York, 1957.

TRANSISTOR LIMITATIONS

6-1 VOLTAGE LIMITATIONS

A number of device constraints limit the designer in the application of transistors. In fact, consideration of device limitations is an integral part of the design of any circuit.

There is a maximum voltage, for instance, beyond which a given transistor will fail to operate properly. Such is the case because internal voltage breakdown will exist, and the device may be destroyed because of the resulting high internal-power dissipation. Depending upon the type of transistor involved, voltage breakdown may be caused by Zener, avalanche, or punch-through effects.

Two junctions are associated with transistors, base-emitter and base-collector. These junctions are similar to two semiconductor diodes connected as shown in Fig. 6-1. Each junction can be tested for opens or shorts with, say, an ohmmeter as if they were separate semiconductor diodes.

Several voltage ratings are usually specified by the manufacturer. The voltage rating V_{CBO} is the collector-to-base rating with the emitter lead open-circuited, and, similarly, V_{CEO} is the collector-to-emitter rating with the base lead open-circuited. The voltage rating for V_{CBO} generally exceeds that for V_{CEO} . For instance, a typical silicon-epitaxial planar transistor has a specified V_{CBO} rating of 25 V and a V_{CEO} rating of 15 V. That is, the collector-to-base voltage should never be allowed to exceed 25 V with the emitter lead open-circuited, and the collector-to-emitter voltage should never be allowed to

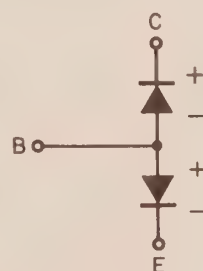


FIG. 6-1 Diode Equivalent for an NPN Transistor

exceed 15 V with the base lead open-circuited. If a resistor is connected from B to E in the circuit of Fig. 6-1, the collector-to-emitter breakdown voltage (V_{CER}) will be a value between V_{CEO} and V_{CBO} . The V_{CER} rating for the aforementioned transistor is 20 V with a $10\text{-}\Omega$ resistor connected between base and emitter.

When a transistor is operated in the active region (neither cutoff nor saturated), the base-emitter diode is forward biased, and the base-collector diode is reverse-biased. However, in switching circuitry, the base-emitter diode may be reverse biased to switch the transistor to the cutoff state. The ratings V_{CBO} , V_{CEO} , and V_{CER} refer to the base-collector diode, and a reverse breakdown rating for the base-emitter diode must also be specified. The V_{EBO} rating for the aforementioned NPN transistor is 5 V. That is, if the emitter is positive with respect to the base, the base-emitter diode is reversed biased, and, if the magnitude of the bias exceeds 5 V, voltage breakdown may occur.

Transistor junctions are not necessarily destroyed by operation in the breakdown mode. In switching circuitry, the base-emitter diode is sometimes operated in the breakdown region, but the reverse current is always limited to ensure that junction power dissipation is not excessive.

6-2 POWER LIMITATIONS

A necessary result of power dissipation in a transistor is a rise in junction temperature. It is primarily maximum allowable junction temperature which constrains power dissipation. Maximum junction temperature for germanium transistors is of the order of 100°C and for silicon transistors, 150° to 200°C . Beyond these temperatures, degradation of performance or total device failure is likely.

The most significant area of power dissipation is near the collector junction, and heat must be conducted from this junction to the outside world to prevent excessive junction temperatures. Since there is thermal resistance between the transistor junction and case and between the case and free air or external heat sink, junction temperature always exceeds case temperature (for an operating transistor). Transistors are available with power ratings from a few milliwatts to many watts, but, in any case, the designer's problem is to ensure that junction temperatures do not exceed safe limits.

Maximum transistor power dissipation occurs in Class A operation where the collector-to-base voltage V_{CB} is equal to one-half the supply voltage, and the collector current I_c is equal

to one-half the maximum collector current $I_{\max}$. Such is indicated by Eq. (6-1)

$$P_{\max} = \frac{(V_{cc})(I_{\max})}{4} \text{ watts} \quad (6-1)$$

Figure 6-2 illustrates the collector characteristics of a silicon-planar transistor. The maximum constant-power hyperbola is shown with a load line which represents the maximum for Class A operation. This load line is the one which is tangent to the hyperbola and which intersects the abscissa at the collector supply voltage V_{cc} . The value of the load impedance for the case illustrated in Fig. 6-2 is 800Ω , and the maximum allowable collector-power dissipation is 500 mW. Three of the constant base current curves are also shown, and voltage breakdown occurs in the region of points a , b , and c . Since some finite saturation resistance exists, the characteristic curve does not coincide with the y -axis except at the origin. When a transistor is saturated (switched on), the collector-to-emitter voltage is referred to as $V_{CE(SAT)}$ or simply V_{SAT} . The manufacturer usually specifies either saturation voltage or saturation resistance for a particular set of operating conditions.

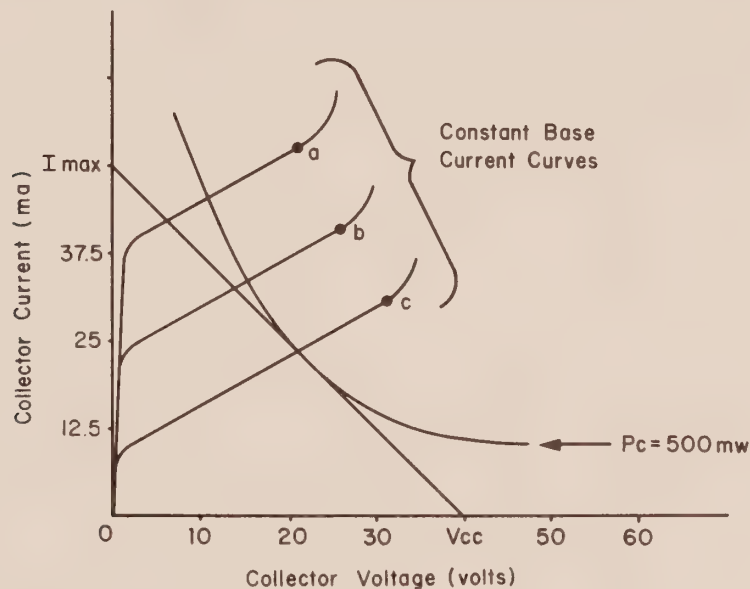


FIG. 6-2 Collector Characteristics

It is possible to operate on a load line in Fig. 6-2 which passes through the maximum-power hyperbola. Such is the case because collector-power dissipation is at a minimum when the transistor is either cutoff or saturated. Power dissipation is

equal to the product of collector voltage and collector current. At saturation, collector voltage is very small, and, likewise, collector current is quite small at cutoff. In switching applications where the transistor is switched rapidly from cutoff to saturation and vice versa, average power dissipation may be negligible, and the transistor is, therefore, capable of switching much greater load currents than the average power rating would indicate.

In power applications, it is standard practice to mount transistors on heat sinks. The value of employing a heat sink is illustrated by the manufacturer's specifications for a particular transistor. In free air at an ambient temperature of 25°C , the stated power rating is 500 mW, but the rating is 1,800 mW at a transistor case temperature of 25°C .

The collector of almost every power transistor is connected electrically to the transistor case. Thus, insulation is often required between transistor case and heat sink, and such may be accomplished with a mica washer. Of course, the mica washer introduces some thermal resistance which results in higher junction temperatures. Another factor which affects junction temperature is temperature rise of the heat sink. Figure 6-3 illustrates the temperature rise coefficient of a square sheet of aluminum, three-sixteenths of an inch in thickness, as a function of heat sink area. An example is best used to illustrate calculations associated with power applications.

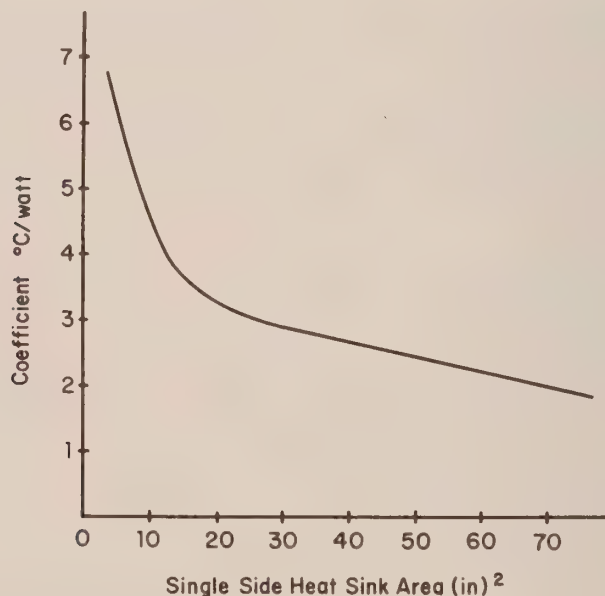


FIG. 6-3 Temperature-Rise Coefficient — Aluminum Heat Sink

Example 6-1

A particular application requires transistor-power dissipation of 10 W, and the transistor case must be electrically insulated from the heat sink. The transistor specifications indicate thermal resistance from junction to case of $1^{\circ}\text{C}/\text{W}$ and maximum allowable junction temperature of 95°C . A heat sink must be designed to allow operation at ambient temperatures to 50°C . For insulation purposes, a mica washer is used, and the stated washer coefficient is $0.6^{\circ}\text{C}/\text{W}$. Equation (6-2) defines the transistor junction temperature T_j in terms of power dissipation P , thermal-resistance coefficients θ_j (junction-to-case), θ_w (insulator), θ_s (heat-sink), and ambient temperature T_a

$$T_j = T_a + P(\theta_j + \theta_w + \theta_s) \text{ }^{\circ}\text{C} \quad (6-2)$$

In this problem, the task is to solve for the heat-sink coefficient θ_s

$$95 = 50 + 10(1 + 0.6 + \theta_s)$$

$$\theta_s = 2.9^{\circ}\text{C}/\text{W}$$

The curve of Fig. 6-3 is then used to find the minimum allowable heat-sink area. The answer is approximately 20 sq in. or a square section of aluminum 4.5 in. by 4.5 in. To establish some design margin, one would probably specify a heat-sink area of 36 sq in. (6×6). Maximum heat-sink temperature T_s , in the case of the larger heat sink ($\theta_s = 2.5^{\circ}\text{C}/\text{W}$), would be 75°C .

Transistor power ratings are frequently specified for free-air applications (no heat-sink) at an ambient temperature of 25°C . The power rating at elevated temperatures is less than the rating at 25°C , and the designer must determine the ratings at temperatures other than room temperature. For free-air applications, the manufacturer usually specifies a derating factor. For instance, a particular transistor with a free-air (25°C) rating of 500 mW is derated by the manufacturer at a rate of $2.86 \text{ mW}/^{\circ}\text{C}$. The allowable power dissipation at, say, 75°C is calculated as follows

$$P_{75} = 500 - 2.86(75 - 25)$$

$$= 357 \text{ mW}$$

6-3 FREQUENCY LIMITATIONS

The constant gain-bandwidth concept in vacuum tube circuitry is valid, at most frequencies of interest, because operating frequency limitations are imposed by RC products rather than by frequency-dependence of the vacuum tube amplification factor μ . Thus, the bandwidth of a given amplifier can be extended by reducing the value of the load impedance, but the stage gain is reduced by an equivalent percentage so that constant gain-bandwidth is maintained.

In a transistorized amplifier, one may not necessarily be able to trade gain for bandwidth and vice versa because transistor current gain (α , β , h_{fe}) is frequency-dependent. The bandwidth of an amplifier can be extended by reducing the magnitude of the load impedance if the upper frequency limit is constrained by an RC product. It is important for high-frequency applications to be able to deduce what effect is controlling amplifier frequency response.

A number of factors affect the high frequency characteristics of a transistor; the most significant from a Circuit Designer's standpoint are input capacitance, collector capacitance, and frequency dependence of current gain. Equation (6-3) expresses a first-order approximation of current gain as a function of frequency

$$\alpha = \frac{\alpha_o}{1 + j \omega / \omega_\alpha} \quad (6-3)$$

Current gain α at the frequency ω is less in magnitude than the low-frequency gain α_o . Furthermore, an imaginary term is involved which results in phase shift at high frequencies. The equation for β as a function of frequency is the same as Eq. (6-3) if α and α_o are replaced by β and β_o , respectively, and ω_α is replaced by ω_β where ω_β is equal to $(1 - \alpha_o) \omega_\alpha$.

Manufacturers specify transistors according to the intended application. For instance, parameters such as rise time, fall time, delay time, collector capacitance, and cutoff frequency f_T are usually specified for transistor types which are intended for switching or video applications. Parameters such as f_{max} , $r'_b C_c$ time constant, input capacitance, output capacitance, and current gain at a given high frequency are specified for communication and high-frequency amplifier transistors. The parameters f_β , f_{max} , and f_T are defined more explicitly as follows: The frequency where the transistor current gain β (or h_{fe}) is equal to 0.707 of its low-frequency value is defined as f_β . The frequency f_{max} is the frequency at which the unilateralized

amplifier power gain is 1. That is, $f_{\max}$ is the maximum frequency of oscillation since an amplifier cannot be made to oscillate if power gain is less than 1. The frequency f_T is the frequency where the forward short-circuit current gain h_{fe} is equal to 1. The gain-bandwidth product of a transistor is, then, equal to f_T . An approximate relationship between $f_{\max}$ and f_T is expressed by Eq. (6-4) and is useful if the manufacturer specifies the $r'_b C_c$ time constant

$$f_{\max} = \sqrt{\frac{f_T}{8\pi r'_b C_c}} \text{ cps} \quad (6-4)$$

Since power gains greater than unity are possible with current gains less than unity, the frequency $f_{\max}$ exceeds the frequency f_T . The curve in Fig. 6-4 is an idealized representation of the variation of unilateralized power gain with frequency.

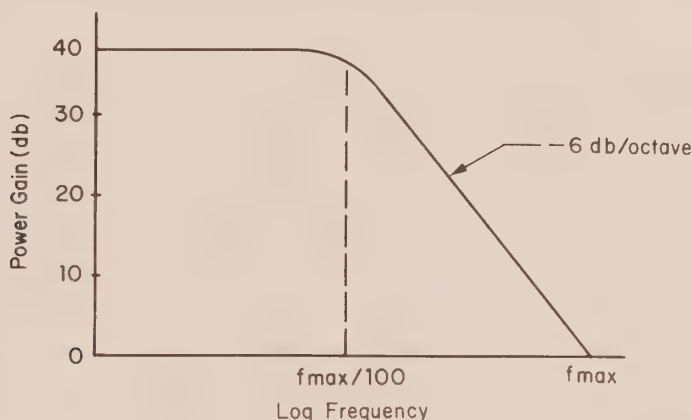


FIG. 6-4 Power Gain vs. Frequency

A decibel (dB) is defined as equal to 10 times the logarithm of power gain or 20 times the logarithm of current or voltage gain. In the high-frequency region, power gain decreases at a rate of 6 dB/octave which is the same as 20 dB/decade. A low-frequency gain of 40 dB is depicted in Fig. 6-4 as a typical value. The indicated breakpoint frequency is $f_{\max}/100$ because the gain reduces from 40 dB to 0 dB in two decades of frequency (20 dB/decade), and two decades reduces to a factor of 100. At the frequency $f_{\max}$, power gain is zero dB or, in absolute terms, 1.

Power gain, in absolute terms, can be calculated from Eq. (6-5) for any frequency between $f_{\max}$ and the cutoff frequency

$$A_p = \left(\frac{f_{\max}}{f} \right)^2 \quad (6-5)$$

Note that power gain in dB is equal to 10 times the logarithm of A_p . Given, for instance, a transistor with an f_{max} of 120 Mc and a β cutoff frequency of 7.5 Mc, Eq. (6-5) can be used to find power gain at any frequency. Table 6-1 illustrates the results. For this example, power gain is limited to 24 dB at frequencies lower than 7.5 Mc.

Table 6-1

Frequency (f)	Power Gain (dB)
120 Mc	0
60	6
30	12
15	18
7.5	24
3.75	24

The curve for β as a function of frequency is similar to that in Fig. 6-4. Two cases are illustrated in Fig. 6-5: a high- β transistor and a low- β transistor where each transistor has the same gain-bandwidth product f_T . It is apparent that the 3-dB point for the low- β transistor exceeds the same point of the high- β transistor. The implication is that, in certain cases, low- β transistors may be preferable to high- β transistors if the gain-bandwidth products are the same.

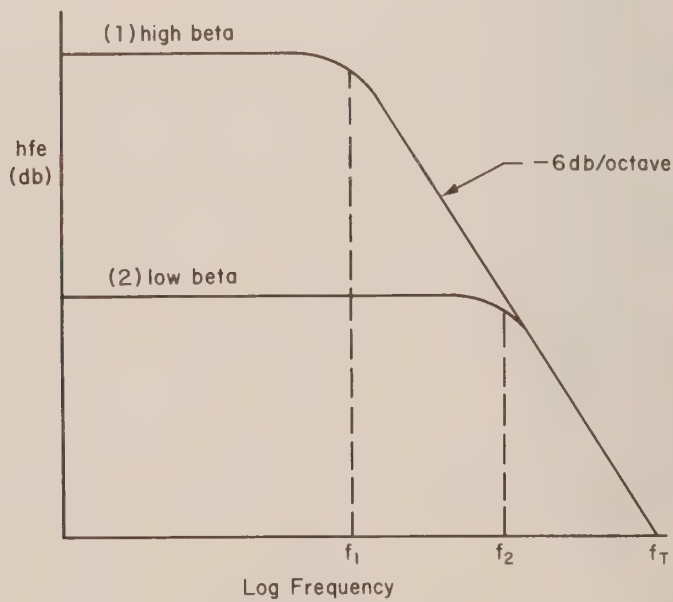


FIG. 6-5 Current Gain (h_{fe}) vs. Frequency

Given an amplifier where the frequency response is limited by a reduction in current gain, Eq. (6-3) can be used in conjunction with Eqs. (5-40) and (5-44) to find voltage gain at any frequency. It is assumed that other transistor parameters are not changing as a function of frequency. This assumption, although not valid, is permissible for simple designs.

If frequency response is limited by collector capacitance C_c , the breakpoint frequency can be found approximately from Eq. (6-6) where A_i is defined for the common-emitter amplifier by Eq. (5-30)

$$f_2 = \frac{1}{2\pi A_i R_L C_c} \text{ cps} \quad (6-6)$$

At frequencies greater than f_2 , amplifier-gain reduces at a rate of 6-dB per octave.

Example 6-2

The amplifier of Fig. 6-6 is to be analyzed for frequency response. The transistor parameters are specified as follows:

$$h_{fe} = 100$$

$$h_{oe} = 10^{-5}$$

$$C_c = 1.4 \text{ pf}$$

$$f_\alpha = 45 \text{ Mc}$$

The reactances of the coupling and bypass capacitors are negligible at the frequencies of interest. The cutoff frequency is calculated from Eq. (6-6)

$$\begin{aligned} f_2 &= \frac{10^{12}}{(2\pi)(91)(1.4)(10^4)} \\ &= 125 \text{ kc} \end{aligned}$$

Since the β cutoff frequency is approximately 450 kc, the predicted amplifier cutoff frequency is 125 kc.

$$f_2 = 125 \text{ kc} \quad \text{Calculated}$$

$$f_2 = 117 \text{ kc} \quad \text{Measured}$$

Frequency response can be optimized such that the β cutoff frequency and the RC cutoff frequency are the same. However, where both effects are present, amplifier gain reduces at a rate of 12-dB per octave.

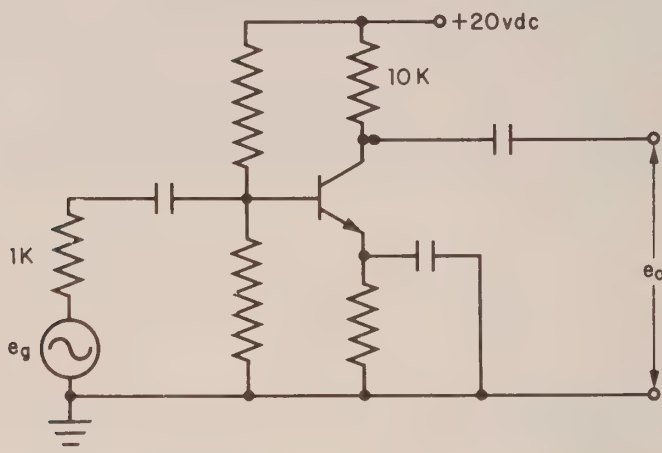


FIG. 6-6 Amplifier Frequency Response

6-4 CURRENT GAIN

As indicated in Sec. 6-3, current gain is a function of frequency. It is also a function of other parameters such as collector current, collector-to-emitter voltage, and temperature. Except for the region near saturation, current gain does not vary drastically with variations in collector-to-emitter voltage. The specifications of a given transistor type, for instance, indicate a current gain variation of plus ten percent for a variation of V_{ce} from 5 V to 25 V. Current gain as a function of temperature and collector current is indicated for a switching transistor by the graphs in Fig. 6-7.

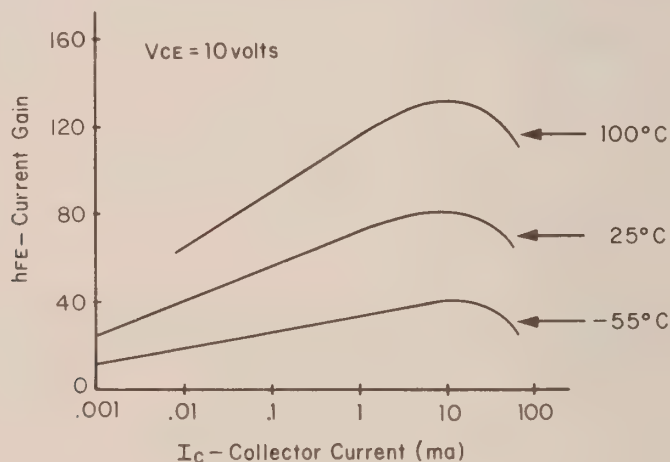


FIG. 6-7 Current Gain vs. I_C and T

Current gain is quite temperature-dependent; it is approximately one-half the room temperature value at -55°C . Although h_{FE} increases at high temperatures, the usual circuit-design problem associated with current gain is at cold temperatures because of the lower gains at such temperatures.

Figure 6-7 indicates a considerable variation in current gain vs. collector current, but it should be noted that a range in collector current from 0.001 mA to 100 mA is quite large. In fact, it is a well-designed switching transistor which maintains a respectable value of current gain at the extremes of collector current shown in Fig. 6-7.

Transistors which are designed for amplifier applications (rather than switching) exhibit h_{FE} vs. I_c characteristics which are considerably inferior to the characteristics depicted in Fig. 6-7. Such transistors are intended to be utilized at particular operating points such as 1 mA or 5 mA for small-signal types. Current gain decreases quite rapidly as the operating point is moved either way from the optimum value of I_c .

One might conclude that switching transistors are superior for all applications, but such is not the case. Transistors which are designed for voltage amplification possess more linear characteristics which facilitate distortionless amplification. Switching transistors, on the other hand, exhibit an output signal which is a nonlinear reproduction of the input signal. That is not to say that the output signal is grossly distorted; the switching transistor is merely inferior to the amplifier transistor in this respect.

6-5 TEMPERATURE EFFECTS

One of the more significant problems confronting the Circuit Designer is the task of designing circuits which function properly over wide temperature ranges. The problem is compounded because of temperature-dependence of transistor characteristics.

Two major temperature-dependent parameters which have not yet been discussed are collector-leakage current I_{co} and base-emitter voltage V_{BE} . The collector-base diode of a transistor is normally operated with a dc-reverse bias, and, if the diode were ideal, no leakage current would occur. However, some reverse leakage current is present, and this current is referred to as I_{co} . The magnitude of I_{co} is a function of the magnitude of the reverse voltage, particularly so where power transistors are involved. Leakage current is also a function of junction temperature. Total leakage current I_{co} can be considered equal to the sum of a voltage-dependent component and

a temperature-dependent component. Manufacturers usually specify I_{co} at the maximum collector-to-base voltage and at both room temperature and some elevated temperature. A curve of I_{co} vs. temperature may also be included. The low-voltage, room-temperature value of I_{co} doubles for approximately every 10°C rise in junction temperature as indicated by Eq. (6-7).

$$(I_{co})_T = (I_{co})(2)^{\Delta T/10} \mu\text{A} \quad (6-7)$$

where $(I_{co})_T$ equals the value of leakage current at the temperature T .

I_{co} equals the low-voltage, room temperature leakage current (μA).

ΔT equals the change in temperature in deg C.

For example, if I_{co} of a given transistor equals $1 \mu\text{A}$ at 25°C , it will increase to $8 \mu\text{A}$ at 55°C .

It is preferable to use the manufacturer's leakage data, if available, rather than Eq. (6-7)—particularly so if germanium power transistors are involved.

The base-emitter diode characteristic of a transistor is similar to that of a semiconductor diode. That is, voltage across the junction increases nonlinearly as the current through the diode is increased linearly (in the forward-biased direction). The base-emitter junction is normally operated in the forward-biased condition. In fact, if the base lead is connected to the emitter lead so that base current I_B is zero, the collector current will essentially be reduced to the leakage current I_{co} . In other words, under zero bias conditions, transistor operation is in the cutoff region. Plate current in a vacuum tube, on the other hand, is quite large for zero grid-cathode bias. A vacuum tube is switched off by reverse bias, and a transistor is switched on by forward bias.

The base-to-emitter voltage drop of silicon transistors is approximately 0.6 V at 25°C and at very low values of base current. At the maximum allowable value of base current, V_{BE} may increase to approximately 1 V . The corresponding values for germanium transistors are 0.15 and 0.4 V . These numbers are, of course, for reference only. The actual voltage limits depend upon transistor type: small-signal, power, etc.

For any given transistor which is operating with a given value of base current, a value of V_{BE} will exist. As the transistor junction temperature is increased, this magnitude of V_{BE} will decrease at a rate of approximately two millivolts per degree

centigrade. The rate of change in V_{BE} ($-2 \text{ mV}/^\circ\text{C}$) is approximately the same for both silicon and germanium transistors.

As junction temperature is increased, the resulting variations in I_{co} and V_{BE} cause an increase in collector current. Depending upon the particular transistor operating point, the increase in collector current may cause additional junction power dissipation which then results in yet higher junction temperatures. A condition which is referred to as *thermal runaway* may then occur, and the transistor may be destroyed.

6-6 DESIGN EXAMPLE

An inexpensive, single-stage audio amplifier is to be designed to drive a $3.2\text{-}\Omega$ load. The frequency range is 150 cps to 15 kc, and the maximum desired output power is 6 W. Also, the signal generator output impedance is equal to $300\ \Omega$. An insertion power gain of approximately 12 dB is desired, but some sacrifice in gain can be tolerated in the interest of economy. The supply voltage is from a 12-V battery, and the expected ambient temperature range is from 0°C to $+55^\circ\text{C}$.

A preliminary sketch (Fig. 6-8) of a configuration which utilizes a PNP power transistor is made, and a transistor is selected with the following characteristics:

$$h_{FE} = 30$$

$$P = 150 \text{ W at } 25^\circ\text{C case temperature}$$

$$I_{CBO} = 100 \text{ }\mu\text{A at } 25^\circ\text{C}$$

$$BV_{CEO} = 55 \text{ V}$$

$$(T_j)_{\max} = 100^\circ\text{C}$$

$$\theta_{JC} = 0.5^\circ\text{C/W}$$

$$f_\beta = 10 \text{ kc}$$

$$V_{CE(sat)} = 0.3 \text{ V at } I_c \text{ equal to } 12 \text{ A}$$

Transformer output is assumed, and a transformer with a two-to-one turns ratio, primary dc resistance of $1\ \Omega$, and secondary dc resistance of $0.3\ \Omega$ is selected. The ac output current is calculated as follows

$$\begin{aligned}
 I_o^2 &= \frac{P_o}{R_L} \\
 &= \frac{6}{3.2} \\
 &= 1.37 \text{ A rms}
 \end{aligned}$$

The ac primary current is equal to $I_o/2$ because of the transformer 2:1 turns ratio

$$\begin{aligned}
 I_{pr} &= \frac{1.37}{2} \\
 &= 0.685 \text{ A rms} \\
 &= 0.97 \text{ A pk}
 \end{aligned}$$

The transformer primary current must swing to a positive peak of 0.97 A and also to a negative peak of 0.97 A. That is, the peak-to-peak current swing is almost 2 A. Therefore, the transistor dc collector current must be 1 A or greater to allow the primary current to decrease by 1 A when the transistor is driven toward cutoff. Thus, the dc operating-point current is set at 1 A, and the required dc base current is equal to 1 A divided by the transistor current gain

$$I_B = \frac{1}{30} \text{ A}$$

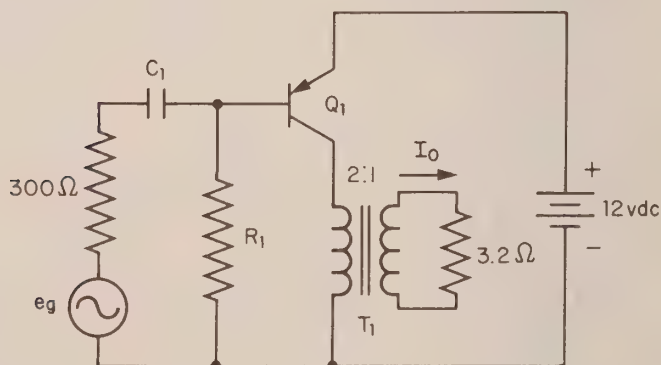


FIG. 6-8 Audio Amplifier

The voltage across resistor R_1 is equal to $(12 - V_{eb})$ V or approximately 12 V since the transistor emitter-base voltage

is small. A value for R_1 can now be calculated

$$\begin{aligned} R_1 &= \frac{12}{1/30} \\ &= 360 \quad \Omega \end{aligned}$$

A value for capacitor C_1 can be calculated from Eq. (5-24) if one assumes that the amplifier input impedance is approximately equal to the value of R_1

$$\begin{aligned} C_1 &= \frac{1}{2\pi f_1 (R_o + R_i)} \\ &= \frac{1}{(2\pi)(150)(300 + 360)} \\ &= 1.6 \mu\text{F} \end{aligned}$$

A tantalum-type capacitor with a standard value of $1.8 \mu\text{F}$ is selected.

It would appear that the design is complete. All component values have been determined, and a 150-W transistor has been selected. However, certain important amplifier parameters are still unknown. What is the insertion power gain, the frequency response, full-output distortion, and transistor power dissipation?

Transformer regulation must be determined because it affects insertion gain and signal amplitude at the transistor collector which in turn affects signal distortion. An equivalent circuit of the transformer consists of a signal generator with an amplitude of one-half the primary voltage in series with the load resistor (3.2Ω), the secondary dc resistance, and the reflected primary dc resistance. See Fig. 6-9. The transformer turns ratio 1:n is equal to 1:0.5, and the primary dc resistance is reflected to the secondary by the square of the turns ratio. Hence, the resistors in the equivalent circuit are equal to 0.25, 0.3, and 3.2Ω . The approximate power lost in the transformer is as follows

$$\begin{aligned} P_L &= (I_o)^2(R_o) \\ &= (1.37)^2(0.55) \\ &= 1.03 \text{ W} \end{aligned}$$

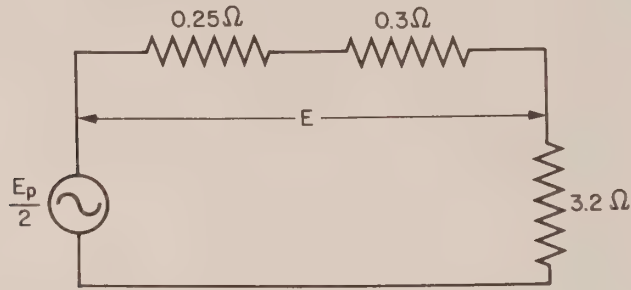


FIG. 6-9 Transformer Equivalent Circuit

Transformer efficiency is equal to power out divided by power out plus losses.

$$\begin{aligned}\eta &= \frac{P_o}{P_o + P_L} \\ &= \frac{6}{6 + 1.03} \\ &= 85\%\end{aligned}$$

Full-load current is equal to 1.37 A rms which causes a voltage drop across the transformer output resistance.

$$\begin{aligned}E &= (1.37)(0.55) \\ &= 0.75 \text{ vrms}\end{aligned}$$

The full-load voltage across the 3.2-Ω resistor is as follows:

$$\begin{aligned}E_o &= (1.37)(3.2) \\ &= 4.38 \text{ vrms}\end{aligned}$$

The full-load primary voltage is:

$$\begin{aligned}E_{pr} &= 2(0.75 + 4.38) \\ &= 10.26 \text{ vrms} \\ &= 14.5 \text{ V peak}\end{aligned}$$

For full-output power, the peak primary voltage is 14.5 V. The dc voltage drop across the primary winding is equal to

1 A multiplied by $1\ \Omega$ (1 V). In addition, the transistor saturation voltage is greater than 0, say 0.1 V. It is apparent that the desired signal swing is unattainable with the described circuit and a 12-V supply voltage. That is, the positive signal peak is going to be clipped to a value less than 12 V. The result of such operation is signal distortion and a reduction in output sound fidelity. Nevertheless, this deficiency is not considered sufficient cause to expand the design.

Power gain is calculated with the assumption that the amplifier input impedance is equal to the magnitude of the input resistor R_1 (360 Ω). The ac input current is found first

$$i_c = 0.685\text{ A rms}$$

$$i_b = \frac{0.685}{30}$$

$$= 22.8\text{ mA rms}$$

$$P_{\text{in}} = (i_b)^2 R_1$$

$$= 187\text{ mW}$$

$$P_g = \frac{P_o}{P_{\text{in}}}$$

$$= \frac{6}{0.187}$$

$$= 32$$

$$\text{dB} = 10 \log P_g$$

$$= 15$$

Power gain from transistor input to output load resistor is 15 dB, but this is not the insertion power gain because some power is lost in the 300- Ω generator impedance. The lost power is

$$P_{300} = (22.8)^2 (300) (10^{-6})$$

$$= 156\text{ mW}$$

Thus, the signal generator is delivering 156 plus 187 mW for a total input power of 343 mW. The insertion power gain is

$$P_g = \frac{6}{0.343}$$

$$= 17.5$$

$$= 12.4 \text{ dB}$$

The insertion power gain including transformer losses is 12.4 dB assuming linear amplifier operation (no signal limiting).

Amplifier frequency response is easily calculated if the transformer bandwidth is large with respect to the desired frequency range (150 cps to 15 kc). The transistor β cutoff frequency was specified as 10 kc which means that gain is down 3dB at 10 kc and decreasing at a rate of 6 dB per octave. In other words, the amplifier high-frequency cutoff point, f_2 , is 10 kc rather than 15 kc. The frequency response would not be considered hi-fidelity, but it would possibly be adequate.

The last major area of interest is transistor power dissipation. Since a Class A amplifier is involved, transistor power dissipation is equal to the dc collector current multiplied by the dc collector-emitter voltage. The collector current is 1 A, and the voltage drop across the transformer primary is 1 V; so the collector-emitter voltage is 11 V. Collector dissipation is then equal to 11 W. Pertinent power information is rewritten here

$$P = 150 \text{ W at } 25^\circ\text{C case temperature}$$

$$(T_j)_{\max} = 100^\circ\text{C}$$

$$\theta_{JC} = 0.5^\circ\text{C/W}$$

$$(T_a)_{\max} = 55^\circ\text{C}$$

Assuming use of a heat sink with a coefficient of θ_s $^\circ\text{C/W}$, the junction temperature is expressed as follows:

$$T_j = T_a + 11(\theta_{JC} + \theta_s)$$

$$100 = 55 + 11(0.5 + \theta_s)$$

The maximum heat-sink coefficient is 3.6°C/W , and the required heat-sink area is found from Fig. 6-3 to be approximately

13 sq in. This is assuming that electrical insulation between transistor and heat sink is not required.

Some observations about the design are appropriate. The frequency response is poor, signal distortion occurs at full output, efficiency is poor, and the transformer is operated with an undesirably large dc primary current. Furthermore, the dc operating point current is a direct function of transistor β which varies from transistor to transistor and with junction temperature. The amplifier is, however, inexpensive, and this factor may dominate the design. A more common approach for satisfying the stated design requirements is to employ a Class B rather than a Class A amplifier.

PROBLEMS

- 6-1 If the low-frequency current gain of a transistor is 100 and the β cutoff frequency is 500 kc, what is the current gain at 1.2 Mc?
- 6-2 a. Given the dc operating point of a Class A amplifier as $V_{CE} = 10$ V and $I_c = 50$ mA, what is the transistor power dissipation?
b. What is the magnitude of the collector supply voltage?
c. If the transistor were driven to saturation, what would be the collector current?
- 6-3 How many square inches of heat sink area is required for an amplifier which is dissipating 12 W in the output transistor where θ_{JC} is $1^\circ\text{C}/\text{W}$, $(T_{j'})_{\text{max}}$ is 100°C ? Assume that the transistor need not be electrically insulated from the heat sink. The ambient temperature is 52°C .
- 6-4 a. The low-voltage, room-temperature value of I_{co} for a given transistor is $0.1 \mu\text{A}$. What is the value, approximately, at 125°C ?
b. When the transistor is connected as a linear amplifier, the room-temperature emitter-base voltage is 600 mV. What is the approximate magnitude of this voltage at 125°C ?
- 6-5 The input impedance of an RC-coupled amplifier is $10 \text{ k}\Omega$, and the generator impedance is also $10 \text{ k}\Omega$. What minimum value of coupling capacitor between generator and amplifier is required for a low-frequency cutoff point of 100 cps? Specify a probable design value.
- 6-6 A video amplifier with an upper cutoff frequency of 1 Mc is desired. However, the amplifier is to be exposed to radiation which will degrade transistor characteristics, and it is, therefore, decided that the initial amplifier response should be to 5 Mc. It is determined that the response is to 2 Mc after exposure to radiation. Nevertheless, the desired frequency response is to only 1 Mc before and after radiation exposure. The amplifier output resistance is 500Ω . Propose a method which retains the high-frequency transistors but yet solves the problem.
- 6-7 The following specifications apply to the transistor which is depicted in Fig. 1:

$$V_{CEO} = -20 \text{ V maximum}$$

$$V_{BE} = 6 \text{ V maximum}$$

$$(I_C)_{\max} = 50 \text{ mA}$$

$$(P_C)_{\max} = 400 \text{ mW}$$

$$B = 30$$

- a. What happens with switch S open?
- b. What happens when switch S is closed?

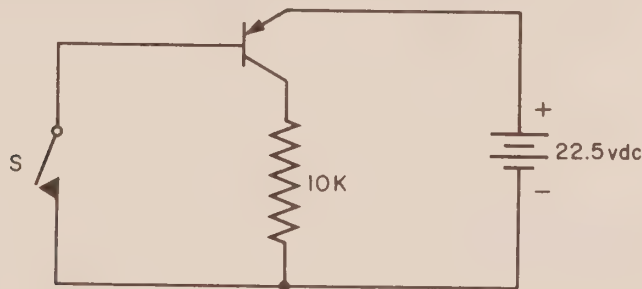


FIG. 1 PNP Amplifier

- 6-8 Figure 2 depicts part of a circuit which is used for pulse-width discrimination. That is, an output from the level detector is required if the input pulse width exceeds a given value. Both transistors are of the same type with the following characteristics:

$$V_{CEO} = 30 \text{ V maximum}$$

$$V_{EB} = 7 \text{ V maximum}$$

$$\beta = 100 \text{ max; } 50 \text{ min}$$

$$t_r = 0.12 \text{ } \mu\text{s typical}$$

$$t_f = 0.3 \text{ } \mu\text{s typical}$$

$$I_C = 150 \text{ mA maximum}$$

$$P = 600 \text{ mW maximum}$$

$$V_{CE(\text{sat})} = 50 \text{ mV maximum}$$

$$I_{co} = 0.1 \text{ } \mu\text{A}$$

An output from the level detector will occur if the detector input voltage is equal to or greater than +12 V. Assume that the detector input impedance is infinite.

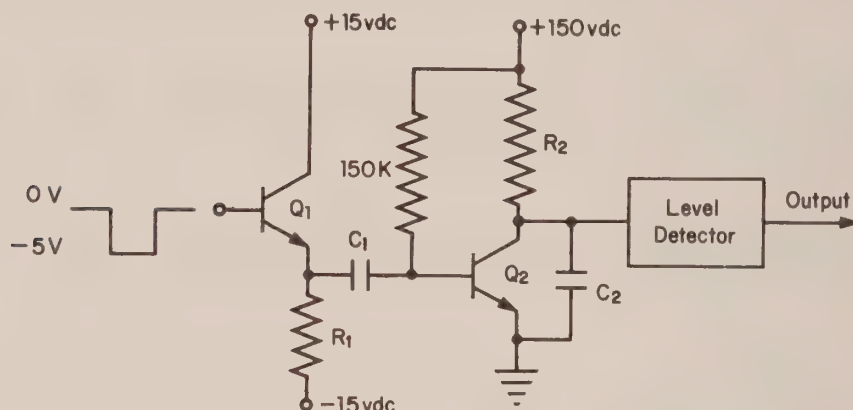


FIG. 2 Pulse-Width Discriminator

The discriminator input signal is from a low-impedance generator, is negative going with a peak amplitude of -5 V , and has a pulse width anywhere within the range of $1\text{ }\mu\text{s}$ to $20\text{ }\mu\text{s}$. An output signal is required if the input pulse width is equal to or greater than $10\text{ }\mu\text{s}$.

Calculate design values for R_1 , R_2 , C_1 , and C_2 . Indicate the minimum allowable values for R_1 and C_1 . What peak voltage occurs at the collector of Q_2 when the input pulse width is equal to $20\text{ }\mu\text{s}$? What is the maximum peak collector current of Q_2 assuming no differentiation of the signal at the base of Q_2 ($I_B = 1\text{ mA}$)? Hint: Approximately 1 mA is conducted through the 150 K resistor at *all* times. The current path is either through the base-emitter diode of Q_2 to ground or through C_1 and R_1 to the negative 15-V supply.

BIBLIOGRAPHY

- GE Staff: "GE Transistor Manual," 7th ed., chap. 2, General Electric, 1964.
- Gray, C., T. Lawson, and L. Weldon: "Transistor Guide for Communications Circuit Designers," Application Lab Report 701B, Philco Corporation, 1963.

OPERATING-POINT STABILIZATION

7-1 DEFINITION OF STABILITY FACTORS

Operating-point considerations are more important in transistor circuitry than inequivalent vacuum-tube circuitry because of the greater temperature dependence of transistor parameters. Furthermore, dc operating point is important in the design of ac amplifiers as well as dc amplifiers.

The designer is concerned with the stability of the dc operating point. That is, in a given amplifier, the operating point varies as a function of temperature, age, transistor parameters, etc. It is obviously necessary for the designer to be able to predict and stabilize operating points.

Parameters which affect the dc collector current of a transistor are dc current gain, V_{BE} , I_{co} , and supply voltage. In fact, if one could write an expression for I_C in terms of these parameters, the problem would essentially be solved because, by taking partial derivatives, one could determine how I_C varies as a function of any of the other parameters. Consider the circuit of Fig. 7-1. An expression for the dc collector current I_C is derived as follows

$$I_C = \alpha I_E + I_{co}$$

$$I_B = I_E - I_C$$

$$= \frac{I_C(1 - \alpha)}{\alpha} - \frac{I_{co}}{\alpha}$$

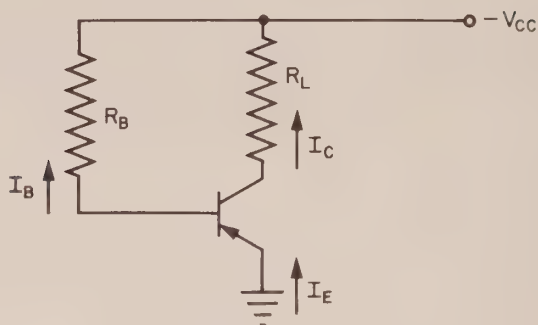


FIG. 7-1 Amplifier Circuit

Writing the two Kirchhoff loop equations

$$1. \quad V_{CC} = I_B R_B + V_{EB}$$

$$2. \quad V_{CC} = I_C R_L + V_{BC} + V_{EB}$$

Solving the two simultaneous equations

$$I_B R_B + V_{EB} = I_C R_L + V_{BC} + V_{EB}$$

$$0 = I_B R_B - I_C R_L - V_{BC}$$

Substituting for I_B and V_{BC}

$$0 = \left[\frac{I_C(1 - \alpha)}{\alpha} - \frac{I_{co}}{\alpha} \right] R_B - I_C R_L - (V_{CC} - I_C R_L - V_{EB})$$

Solving for I_C

$$I_C = \left(\frac{\alpha}{1 - \alpha} \right) \left(\frac{V_{CC}}{R_B} \right) + \frac{I_{co}}{1 - \alpha} - \left(\frac{\alpha}{1 - \alpha} \right) \left(\frac{V_{EB}}{R_B} \right) \quad (7-1)$$

Note:

$$\frac{\alpha}{1 - \alpha} = B = h_{FE}$$

$$\frac{1}{1 - \alpha} = B + 1 = h_{FE} + 1$$

Given an amplifier of the type depicted in Fig. 7-1, one can use Eq. (7-1) to solve for the dc operating current I_C . Furthermore, the sensitivity of I_C to variations in the other parameters can be determined by taking partial derivatives of Eq. (7-1)

$$\frac{\partial I_C}{\partial V_{CC}} = \frac{B}{R_B} \quad (7-2)$$

$$\frac{\partial I_C}{\partial I_{co}} = B + 1 \quad (7-3)$$

$$\frac{\partial I_C}{\partial V_{EB}} = \frac{-B}{R_B} \quad (7-4)$$

Two stability factors are defined as follows:

$$S_C \equiv \frac{\partial I_C}{\partial I_{co}} \cong \frac{\Delta I_C}{\Delta I_{co}} \quad (7-5)$$

$$S_E \equiv \frac{\partial I_C}{\partial V_{EB}} \cong \frac{\Delta I_C}{\Delta V_{EB}} \quad (7-6)$$

For the circuit of Fig. 7-1, the stability factor S_C is determined from Eq. (7-3) to be equal to $B + 1$. This means that, for an incremental change in collector leakage current (ΔI_{co}), the change in collector current is $(S_C)(\Delta I_{co})$ or approximately β times the change in I_{co} .

7-2 THE UNSTABILIZED AMPLIFIER

A Class A amplifier of the type depicted in Fig. 7-1 is designed as an illustrative example. A germanium NPN transistor with the following characteristics is used (see Fig. 7-2)

$$I_{co} = 1 \mu\text{A at } 25^\circ\text{C}$$

$$B = 15$$

$$V_{BE} = 0.25 \text{ V at } 25^\circ\text{C}$$

An operating current of 1 mA is to be established and an analysis made to determine the change in operating current as the ambient temperature is increased to 85°C.

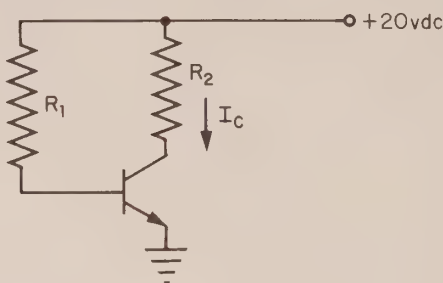


FIG. 7-2 Unstabilized Amplifier

Since the supply voltage is 20 V, and since the operating current is 1 mA, and Class A operation is desired, the value of R_2 in Fig. 7-2 must be 10 k Ω . One can solve for the value of R_1 from Eq. (7-1), but a much simpler method is applicable if it is assumed that I_{co} and V_{BE} are equal to zero

$$\begin{aligned} I_B &= \frac{I_C}{B} = \frac{1}{15} \text{ mA} \\ &= 66.7 \mu\text{A} \\ &= \frac{20}{R_1} \end{aligned}$$

$$R_1 = 300 \text{ k}\Omega$$

If Eq. (7-1) is employed, the answer for the value of R_1 is approximately 302 k Ω . The operating point at 25°C is

$$I_C = 1 \text{ mA}$$

$$V_{CE} = 10 \text{ V}$$

The task is to find the operating point at 85°C

$$\begin{aligned} I_{co} \text{ at } 85^\circ\text{C} &= (1 \mu\text{A}) (2^{\Delta t/10}) \\ &= 64 \mu\text{A} \end{aligned}$$

$$\begin{aligned} \Delta I_{co} &= 64 - 1 \\ &= 63 \mu\text{A} \end{aligned}$$

$$\begin{aligned}
 V_{BE} \text{ at } 85^{\circ}\text{C} &= 250 - 2(\Delta t) \\
 &= 130 \text{ mV}
 \end{aligned}$$

$$\begin{aligned}
 \Delta V_{BE} &= 130 - 250 \\
 &= -120 \text{ mV}
 \end{aligned}$$

The change in collector current is determined from Eqs. (7-3) and (7-4)

$$\begin{aligned}
 \Delta I_C &= (B + 1)(\Delta I_{co}) - \frac{B(\Delta V_{BE})}{R_B} \\
 \Delta I_C &= (16)(63) - \left(\frac{15}{0.3} \right) (-0.12) \mu\text{A} \\
 &= 1.0 \text{ mA}
 \end{aligned}$$

The total collector current at 85°C is equal to the original current plus the change in current

$$\begin{aligned}
 (I_C)_{85^{\circ}} &= (I_C)_{25^{\circ}} + \Delta I_C \\
 &= 2 \text{ mA}
 \end{aligned}$$

It is apparent that the amplifier is in saturation ($V_{CE} \cong 0$) at a temperature of 85°C . The operating point varied primarily because of the increase in collector leakage current I_{co} . If the V_{BE} variation is neglected and it is assumed that β does not vary as a function of temperature, then the total base current at 85°C must be twice the base current at 25°C because the collector current did in fact double. Since the current through the 300 K base resistor is essentially independent of temperature (assuming a temperature-stable resistor type), the additional base current must be due to the increase in collector leakage current.

Transistors are designed to amplify current. If current is conducted from the base to emitter (in an NPN transistor), amplification of that current by the transistor dc beta occurs. The source of the current is of little importance to the point in question. That is, collector leakage current I_{co} is like any other input base current if conduction through the base-emitter diode occurs. Operating-point stabilization is achieved by providing

an additional current path for the collector leakage current so that only a fraction of I_{co} is conducted through the base-emitter diode. A conventional technique is described in Sec. 7-3.

7-3 OPERATING POINT

The circuit of Fig. 7-3 is used to illustrate how an operating point is established and stabilized. The first step is to write an equation for the collector current I_C in terms of I_{co} , V_{BE} , and V_{CC} . If one follows the procedure outlined in Sec. 7-1, Eq. (7-7) results

$$I_C = \frac{I_{co}(1 + R_E/R_1 + R_E/R_2)}{1 - \alpha + R_E/R_1 + R_E/R_2} - \frac{\alpha(1/R_1 + 1/R_2)V_{BE}}{1 - \alpha + R_E/R_1 + R_E/R_2} + \frac{\alpha V_{CC}}{R_1(1 - \alpha + R_E/R_1 + R_E/R_2)} \text{ amperes} \quad (7-7)$$

Let R_{eq} equal the parallel combination of R_1 and R_2 . Then the stability factor S_C is as follows:

$$\begin{aligned} S_C &= \frac{\partial I_C}{\partial I_{co}} \\ &= \frac{1 + R_E/R_{eq}}{1 - \alpha + R_E/R_{eq}} \\ &\cong 1 + \frac{R_{eq}}{R_E} \end{aligned} \quad (7-8)$$

The stability factor S_E is as follows

$$\begin{aligned} S_E &= \frac{\partial I_C}{\partial V_{BE}} \\ &= \frac{-\alpha/R_{eq}}{1 - \alpha + R_E/R_{eq}} \\ &\cong \frac{-\alpha}{R_E} \end{aligned} \quad (7-9)$$

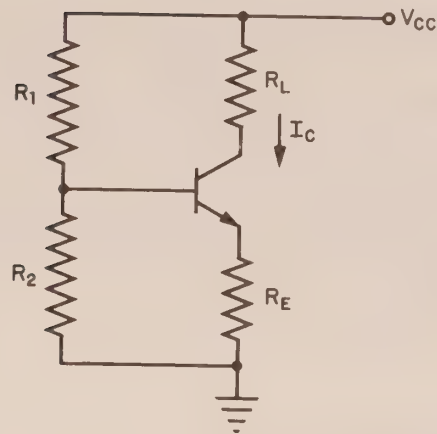


FIG. 7-3 Stabilized Amplifier Circuit

Except for the more critical designs, Eq. (7-8) is sufficient for determining operating-point stability. However, if very low leakage silicon transistors are involved, one may need Eq. (7-9), as well.

Equation (7-7) is normally not used to establish an operating point because it is rather cumbersome and because the terms containing I_{co} and V_{BE} are quite small at room temperature. The following series of steps is usually involved in setting an operating point:

1. Specify the supply voltage (if not already specified) and choose a transistor type.
2. Note the variation of I_{co} over the expected temperature range. Calculate or choose an allowable variation in collector-to-emitter voltage. This change in voltage is approximately equal to the product of the stability factor S_C , the load resistor R_L , and the change in I_{co} . Choose a value for R_L , and solve for the required stability factor S_C which is usually within the range of 3 to 10.
3. At this step the known quantities are: transistor type and all the pertinent characteristics, V_{CC} , R_L , and S_C . The voltage drop across resistor R_E should, in general, be equal to or greater than the magnitude of the base-emitter voltage. Choose a value for R_E and calculate I_C for Class A operation. Alternately, choose an approximate operating current I_C , and specify R_E such that $I_C R_E$ equals about one-tenth the supply voltage.
4. The remaining unknown quantities are resistors R_1 and R_2 . Resistor R_2 is approximately equal to $S_C R_E$ and can be specified as such. Assume that the transistor base current is equal to zero, and calculate resistor R_1 to give a divider voltage which is equal to V_{BE} plus $I_E R_E$.

5. Calculate the required base current at the specified collector current. Assume that the divider R_1 and R_2 is disconnected from the base of the transistor. Calculate a base resistor R_B to supply the required base current. The voltage across R_B is $V_{CC} - V_{BE} - I_E R_E$. Find the parallel value of R_B and R_1 . The result is the final value of the resistor which is connected from transistor base to power supply.
6. Recheck the complete design.

7-4 A STABILIZED AMPLIFIER

An amplifier of the type depicted in Fig. 7-3 is designed by using the suggested procedure of Sec. 7-3. The supply voltage is chosen to be 20 V, and a germanium transistor type is selected. The given characteristics are:

$$I_{co} = 1 \mu\text{A at } 25^\circ\text{C}$$

$$B = 15$$

$$V_{BE} = 0.25 \text{ V at } 25^\circ\text{C}$$

Maximum ambient temperature is 85°C , and the change in I_{co} is $63 \mu\text{A}$ (see Sec. 7-2).

Dynamic range requirements for this particular amplifier indicate that the collector-to-emitter voltage should not vary more than 3 volts as a function of temperature

$$\Delta V_{CE} = (S_C)(\Delta I_{co})(R_L)$$

A suitable value for R_L , as determined from gain and impedance considerations, is $10 \text{ k}\Omega$. One can now solve for S_C

$$\begin{aligned} S_C &\cong \frac{\Delta V_{CE}}{(\Delta I_{co})(R_L)} \\ &= \frac{3}{(63)(10^{-2})} \\ &\cong 5 \end{aligned}$$

The next step is to choose either a value for R_E or an operating current I_C . Let the operating current be 1 mA and the

voltage drop across R_E one-tenth of 20 volts or 2 volts. Resistor R_E is then equal to 2 k Ω .

The values of the base divider resistors R_1 and R_2 are yet to be calculated. One can use the rule of thumb that R_2 is equal to $S_C R_E$ or 10 k Ω , but some additional stabilization margin can be obtained by making R_2 somewhat less than 10 k Ω (at the sacrifice of ac gain). Arbitrarily let the value of R_2 equal 6.2 k Ω . Resistor R_1 can now be calculated to give a divider voltage of $V_{BE} + I_E R_E$

$$V_{BE} + I_E R_E = 0.25 + (1.067)(2)$$

$$= 2.38 \text{ V}$$

$$\frac{2.38}{20} = \frac{R_2}{R_1 + R_2}$$

$$0.119 = \frac{6.2}{R_1 + 6.2}$$

$$R_1 = 46 \text{ k}\Omega$$

A final value for R_1 can be determined after one solves for the base resistor R_B (see Sec. 7-3, step 5)

$$R_B = \frac{20 - 2.38}{67 \mu\text{a}}$$

$$= 262 \text{ k}\Omega$$

$$R_1 = \frac{(46)(262)}{46 + 262}$$

$$\approx 39 \text{ k}\Omega$$

All the component values have been determined, and the operating-point variation as a function of temperature can be predicted

$$S_C = 1 + \frac{R_{eq}}{R_E}$$

$$R_{eq} = \frac{(6.2)(39)}{6.2 + 39}$$

$$= 5.35 \text{ k}\Omega$$

$$S_C = 1 + \frac{5.35}{2}$$

$$= 3.68$$

The variation in I_C as a result of the variation in I_{co} is

$$\Delta I_C = (S_C)(\Delta I_{co})$$

$$= (3.68)(63) \mu a$$

$$= 0.232 \text{ mA}$$

The variation in I_C as a result of the variation in V_{BE} (assuming a coefficient of $-2 \text{ mV}/^\circ\text{C}$) is

$$\Delta I_C = (S_E)(\Delta V_{BE})$$

$$= \left(\frac{-\alpha}{R_E} \right) (-2 \times 60 \times 10^{-3})$$

$$= 0.056 \text{ mA}$$

The total variation at 85°C in the operating current I_C is

$$(\Delta I_C)_T = 0.232 + 0.056$$

$$= 0.288 \text{ mA}$$

The variation in operating-point voltage is

$$\Delta E = -(\Delta I_C)(R_L)$$

$$= -(0.288)(10)$$

$$= -2.88 \text{ V}$$

Calculated and experimental operating-point data are compared in the following table:

	Calculated	Experimental
Operating Point at 25°C	10 V	9.95 V
Operating Point at 85°C	7.12	7.2

7-5 OTHER STABILIZED AMPLIFIERS

The amplifier of Fig. 7-3 is relatively expensive to produce. Besides the input and output coupling capacitors, four resistors and probably a bypass capacitor in parallel with resistor R_E are required. A more economical design may be appropriate if stabilization requirements are not too severe. Such would be the case where large variations in ambient temperature, supply voltage, and transistor current gain are not expected.

The circuit of Fig. 7-4 is applicable for those requirements where the dc load resistor is large in value, say 10 kΩ or greater. An equation for the collector current I_C is written as follows

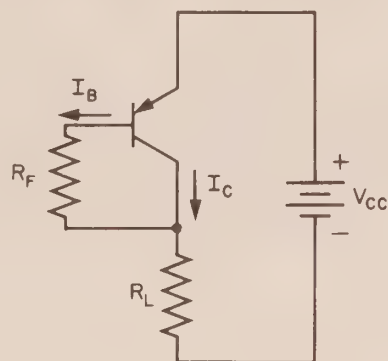


FIG. 7-4 Simple Stabilized Amplifier

$$V_{CC} = V_{EB} + \frac{(1 - \alpha)(R_F + R_L)(I_C)}{\alpha} - (R_F + R_L) \left(\frac{I_{co}}{\alpha} \right) + I_C R_L$$

Solving for I_C

$$I_C = \frac{\alpha(V_{CC} - V_{EB}) + (R_F + R_L)(I_{co})}{(1 - \alpha)R_F + R_L}$$

Taking the partial derivative

$$\frac{\partial I_C}{\partial I_{co}} = \frac{R_F + R_L}{(1 - \alpha) R_F + R_L} \tag{7-10}$$

When one is establishing an operating point, the leakage current I_{co} can be assumed to be zero, and Eq. (7-11) can then be written

$$I_C = \frac{B(V_{CC} - V_{EB})}{R_F + (B + 1)R_L} \quad (7-11)$$

For example, an operating point for the amplifier of Fig. 7-4 is calculated as follows: Let the supply voltage be 20 V, the dc load resistor be 10 k Ω , V_{EB} be 0.6 V, and the transistor current gain be 150 nominal with a minimum to maximum range of 100 to 300. If Class A operation is assumed, the operating point current should be one mA. One can now solve for the value of the feedback resistor from Eq. (7-11)

$$10^{-3} = \frac{150(20 - 0.6)}{R_F + (151)(10^4)}$$

$$R_F = 1.4 \text{ M}\Omega$$

Standard 5 percent resistor values are 1.3 M Ω and 1.5 M Ω . Since maximum β is a greater percentage variation from nominal than minimum β , perhaps 1.5 M Ω is the better choice. The operating point current is calculated for the case where β equals 300

$$I_C = \frac{300(20 - 0.6)}{1.5\text{M} + (301)(10^4)}$$

$$= 1.29 \text{ mA}$$

The operating point voltage has varied from nominal by approximately 3 volts. That is, the magnitude of V_{CE} has changed from 10 volts to 7 volts.

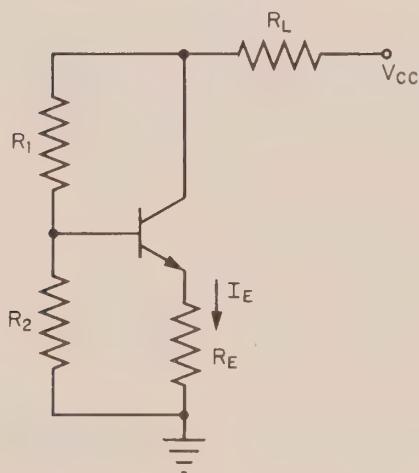


FIG. 7-5 Second Stabilized Configuration

A similar calculation for the minimum β case yields an operating point current of 0.775 mA which results in a voltage variation from nominal of 2.25 volts.

Further operating-point considerations would include resistor tolerance and temperature sensitivity, supply voltage variations, collector leakage current, base-emitter voltage variations, and amplifier dynamic-range requirements.

Second Stabilized-Amplifier Configuration

The circuit of Fig. 7-5 is not often used directly. However, the general equation for I_C or I_E is

quite useful because several different configurations can be described by letting the appropriate resistors equal zero or infinity. For instance, if R_L is equal to zero, the amplifier is an emitter follower. Also, if R_E is equal to zero and R_2 is equal to infinity, the amplifier is the type depicted in Fig. 7-4. The equation for I_E is:

$$I_E = \frac{V_{CC} + R_1 I_{co} - [(R_1 + R_2 + R_L)/R_2](V_{BE})}{(1 + R_E/R_2)(R_1 + R_L) + R_E - \alpha R_1} \quad (7-12)$$

The stability factor is:

$$\frac{\partial I_E}{\partial I_{co}} = \frac{R_1}{(1 + R_E/R_2)(R_1 + R_L) + R_E - \alpha R_1} \quad (7-13)$$

7-6 DESIGN EXAMPLE

An amplifier is to be designed for the following application:

Input signal	100 cps sinusoidal
Voltage gain	200 minimum
Temperature range	0°C to 50°C
Generator impedance	5 kΩ
Load impedance	1 kΩ
Supply voltage	20 vdc
Maximum output voltage	3 V peak

Other considerations include manufacturing cost and amplifier noise. The device is intended for commercial use, and a more simple design is, therefore, preferred. Considerable noise is present in the 100-cps signal at the generating source, and it is desired that the amplifier reject as much noise as possible. However, other considerations dictate that the 100-cps signal not be phase-shifted more than a few degrees, and an amplifier bandwidth of from 10 cps to 1,000 cps is chosen for this reason.

The proposed circuit is depicted in Fig. 7-6, and transistors are selected with the following characteristics:

Transistors Q_1 and Q_3

$$\begin{aligned} h_{FE} &= h_{fe} = 100 \\ h_{ie} &= 4.4 \text{ k}\Omega \end{aligned}$$

$$h_{re} = 7.3 \times 10^{-4}$$

$$h_{oe} = 24 \mu\text{mhos}$$

$$I_{co} = 0.2 \mu\text{A maximum at } 50^\circ\text{C}$$

Transistor Q_2

$$h_{FE} = h_{fe} = 50$$

$$h_{ib} = 30 \Omega$$

$$h_{rb} = 4 \times 10^{-4}$$

$$h_{ob} = 0.2 \mu\text{mho}$$

$$I_{co} = 0.2 \mu\text{A maximum at } 50^\circ\text{C}$$

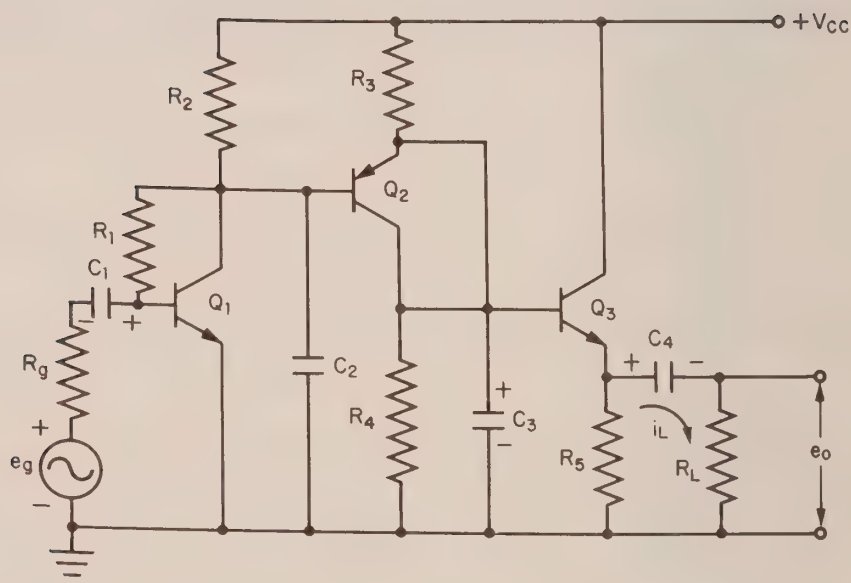


FIG. 7-6 Design-Example Amplifier

Table 5-3 is used to convert the pertinent common-base parameters of Q_2 to common-emitter parameters

$$h_{ie} = 1.5 \text{ k}\Omega$$

$$h_{oe} = 10 \mu\text{mhos}$$

The first step in the design is to set dc operating points starting with transistor Q_3 . For Class A operation, the dc voltage drop across resistor R_5 should be 10 volts. The peak signal

current in R_L is

$$\begin{aligned} i_L &= \frac{\pm 3}{1K} \\ &= \pm 3 \text{ mA} \end{aligned}$$

For reasons described in Sec. 8-5, the dc current through resistor R_5 must exceed the peak load current (3 mA in this case). Let the Q_3 operating current be 10 mA. Resistor R_5 is readily calculated to be 1 k Ω . Also, the voltage at the base of Q_3 is: $V_{B3} = I_E R_5 + V_{BE}$ or approximately 10.6 volts. The Q_3 base current is equal to I_E divided by $(B + 1)$ or approximately 1/10 of a milliamper

$$I_{B3} = 0.1 \text{ mA}$$

Biasing of transistor Q_2 is considered next. It is already known that the magnitude of the collector voltage is 10.6 V and that the supply voltage is 20 V. Also, the specifications indicate the maximum output voltage to be 3 volts peak. Since the voltage gain of the emitter follower (Q_3) is approximately 1, the dynamic range at the collector of Q_2 is ± 3 volts. In other words, the collector of Q_2 must be allowed to swing to 13.6 V or, say, 14 V. The dc voltage at the emitter of Q_2 should be equal to or greater than 14 V to ensure the desired amplifier dynamic range. However, the collector voltage of Q_1 is approximately equal to the emitter voltage of Q_2 , and it is obviously undesirable for the dc collector voltage of Q_1 to approach 20 volts. Thus, a value of between 14 and 20 volts must be selected for the dc operating point at the emitter of Q_2 , and 15 V is hereby selected. The collector voltage of Q_1 is, then, equal to 14.4 volts.

To complete the design of the Q_2 stage, some parameter must be chosen and the others calculated. For instance, one could select a quiescent current and solve for the values of R_3 and R_4 , or select R_4 (or R_3) and solve for the other parameters. If operating-point current is to be chosen, one would probably select a value approximately 10 times the Q_3 base current or 1 mA. If R_4 is to be chosen, then one would probably want to know the approximate input impedance of the Q_3 stage

$$\begin{aligned} (R_{in})_3 &= B \left(\frac{R_5 R_L}{R_5 + R_L} \right) \\ &= (100)(500) \\ &= 50 \text{ k}\Omega \end{aligned}$$

It is desirable to keep the amplifier dc gain low to minimize operating-point variations, and such can be accomplished by choosing a low value for R_4 .

It would appear, in this case, that the best procedure would be to choose an operating-point current for Q_2 of 1 mA. Since the voltage drop across R_4 is 10.6 volts, a value for R_4 is readily calculated to be approximately 10 k Ω (a standard 5-percent value). A value can also be calculated for resistor R_3 :

$$\begin{aligned} R_3 &= \frac{5 \text{ V}}{1 \text{ mA}} \\ &= 5 \text{ K} \end{aligned}$$

A standard 5-percent value is 5.1 k Ω . Note that the dc voltage gain of the Q_2 stage is approximately 2.

Biasing for the Q_1 stage is considered next, and the operating-point voltage is already known.

$$\begin{aligned} V_{C1} &= 15 - 0.6 \\ &= 14.4 \text{ V} \end{aligned}$$

The ac input impedance of the Q_2 stage is approximately 1.5 k Ω and one might reason that the output impedance of the Q_1 stage should be the same. Such could be accomplished by choosing a value for R_2 of about 1.5 k Ω . The supposed logic of this course is to match impedances, thereby maximizing amplifier power gain. If transformer coupling were used between stages Q_1 and Q_2 , one could indeed match impedances with the desired improvement in gain. It is a false assumption, however, that gain is maximized by making the value of R_2 equal to the input impedance of the Q_2 stage. This subject is considered in more detail in Sec. 8-1.

In the proposed design, it is desirable to make resistor R_2 as large in value as is practical to maximize gain. The Q_2 dc base current is about 20 μ A, and the Q_1 collector current should be considerably greater because beta is quite low at such collector currents. However, one could arbitrarily say that the minimum value of R_2 should be 10 k Ω for effective bias stabilization. Let the value of R_2 be 20 k Ω . Then the Q_1 collector current is:

$$\begin{aligned} I_{C1} &= \frac{20 - 14.4}{20 \text{ K}} \\ &= 0.28 \text{ mA} \end{aligned}$$

The Q_1 collector current is greater by an order of magnitude than the Q_2 base current, and such is considered satisfactory. A value is computed for R_1 as follows:

$$\begin{aligned} R_1 &= \frac{14.4 - 0.6}{280/100} \\ &= 4.9 \text{ M}\Omega \end{aligned}$$

Let the value of R_1 be 4.7 M Ω .

The coupling and bypass capacitors are considered next. The indicated amplifier bandwidth is 10 cps to 1,000 cps, and the gain at other frequencies should decrease as the input signal frequency is varied beyond 1,000 or below 10 cps. The low-frequency rolloff point can be set by the proper choice of C_1 , C_3 , or C_4 . The upper-frequency rolloff point is set by the choice of C_2 . Since only one high-frequency breakpoint is to be set, one low-frequency breakpoint should also be set to minimize total amplifier phase shift at 100 cps.

Capacitor C_3 may be a logical choice for setting the low-frequency breakpoint because bypass capacitors tend to be large in value and size. The minimum value can then be selected for C_3 . One could calculate as follows

$$\begin{aligned} C_3 &= \frac{1}{\omega R_3} \\ &= \frac{1}{(20\pi)(5.1K)} \\ &= 3.1 \mu\text{F} \end{aligned}$$

However, the $R_3 C_3$ breakpoint is where the stage gain is 3 dB greater than the corresponding dc gain rather than 3 dB less than the mid-frequency gain. The mid-frequency voltage gain is approximately

$$A_v = \frac{-h_{fe} R_L}{h_{ie}}$$

At the breakpoint frequency f_1 , the voltage gain (assuming $R_3 \gg X_C$) is

$$0.707 A_v \angle 45^\circ = \frac{-h_{fe} R_L}{h_{ie} + (h_{fe} + 1)(-j X_C)}$$

If one divides the two equations and solves for the magnitude of X_C , Eq. (7-14) is the result

$$X_C = \frac{h_{ie}}{h_{fe} + 1} \text{ ohms} \quad (7-14)$$

The solution for the given problem is

$$\begin{aligned} X_C &= \frac{1.5 \text{ K}}{51} \\ &= 30 \Omega \end{aligned}$$

The magnitude of capacitance required is

$$\begin{aligned} C &= \frac{1}{(20\pi)(30)} \\ &= 560 \mu\text{F} \end{aligned}$$

The high-frequency breakpoint is set by the selection of C_2 . However, the impedance at the collector of Q_1 must be found first. The input impedance of Q_2 is 3 k Ω , and the output impedance of Q_1 is approximately R_2 in parallel with $1/h_{oe}$. Thus, the impedance at the collector of Q_1 is

$$\begin{aligned} R_{o1} &= \frac{1}{1/1.5\text{K} + 1/20\text{K} + 24(10^{-6})} \\ &= 1.35\text{K ohms} \end{aligned}$$

A value for C_2 is calculated as follows

$$\begin{aligned} C_2 &= \frac{1}{\omega R} \\ &= \frac{10^{-3}}{(2\pi)(1000)(1.35)} \\ &= 0.118 \mu\text{F} \end{aligned}$$

A standard value is 0.12 μF .

Coupling capacitors C_1 and C_4 are considered next. Physical size and unit cost are usually the dominant factors in the selection of coupling capacitors. It is ordinarily undesirable for these capacitors to introduce attenuation and phase shift, however. Let the breakpoint frequency be 5 cps, an octave below the amplifier low-frequency cutoff point

$$\begin{aligned} C_1 &= \frac{1}{\omega(R_g + R_{in})} \\ &= \frac{1}{10\pi(5K + 4.4K)} \\ &= 3.38 \mu F \end{aligned}$$

Let the value of C_1 be $3.3 \mu F$.

A value is calculated for C_4 after assuming that the Q_3 output impedance is much less than R_L (1 k Ω):

$$\begin{aligned} C_4 &= \frac{1}{(10\pi)(1K)} \\ &= 31.8 \mu F \end{aligned}$$

Let the value of C_4 be $33 \mu F$.

DC Operating-Point Stability

One need only calculate the variation in the operating point of Q_1 because the dc voltage gain of Q_2 is quite obviously 2 and the like gain of Q_3 is 1. Equation (7-10) is used to find the operating-point variation of the first stage. Note that R_2 is not the total dc load resistance for Q_1 because of the direct-coupling connection. The dc input impedance of Q_2 is approximately 250 k Ω ($B R_3$). The parallel combination of 250 K and 20 K is 18.5 k Ω .

The change in I_{c_o} from the room-temperature value is 0.2 μA maximum at 50°C assuming that the actual room-temperature value is essentially zero. Thus, the change in collector current is:

$$\begin{aligned} \Delta I_C &= \left(\frac{4.7M + 18.5K}{4.7M/101 + 18.5K} \right) (0.2 \mu A) \\ &= 14.5 \mu A \end{aligned}$$

The change in the Q_1 collector voltage is:

$$\begin{aligned}\Delta E &= (14.5)(18.5)(10^{-3}) \\ &= 0.268 \text{ V}\end{aligned}$$

If one includes the effect due to temperature dependence of V_{BE} , then the total variation is approximately 0.28 V.

The dc voltage gain of the second stage is 2 and of the last stage, 1. Hence, the operating point at the emitter of Q_3 shifts +0.56 volt.

Voltage Gain

The ac voltage gain (at 100 cps) was specified as 200 minimum. For comparison to the specification, it is sufficient to find the approximate nominal gain. Equation (5-44) is rewritten as follows

$$A_v = \frac{-h_{fe}}{(R_{in} + R_T)(Y_L + h_{oe})}$$

The impedance at the collector of Q_1 was found to be 1.35 k Ω , but this includes h_{oe} . That is

$$Y_L + h_{oe} = \frac{1}{1.35 \text{ K}}$$

Therefore, the gain of the first stage is

$$\begin{aligned}A_{v1} &= \frac{-(h_{fe})(1.35\text{K})}{R_{in} + R_T} \\ &= \frac{-(100)(1.35\text{K})}{4.4\text{K} + 5\text{K}} \\ &\cong -14\end{aligned}$$

The input impedance of Q_3 is approximately 50 k Ω . The ac load impedance for Q_2 is the parallel combination of 50 K and 10 k Ω or 8.33 k Ω . The gain is found from Eq. (5-41)

$$\begin{aligned}A_{v2} &= \frac{-(50)(8.33\text{K})}{(51)(30)} \\ &= -270\end{aligned}$$

Note that the output impedance of the Q_1 stage is not included as generator impedance when computing the Q_2 -stage gain because the Q_2 input impedance was included as part of the ac load impedance for the Q_1 stage. Hence, the Q_1 voltage gain was computed to the base of Q_2 .

The output impedance of Q_3 is approximately 100 ohms not including dc load resistor R_5 . The total ac load resistance for Q_3 is 500 ohms, and the voltage gain is, then, 5 divided by 6 or 0.83.

Total amplifier voltage gain is the product of the three stage gains

$$A_{VT} = (14)(270)(0.83)$$

$$\cong 3000$$

Some comments about the design are appropriate. The object of the example is to illustrate how one establishes operating points, controls bandpass characteristics, and calculates multi-stage gains. The final design is not necessarily the optimum for the described application. For instance, a two-stage amplifier would suffice.

An actual design would require the consideration of resistor tolerance, resistor temperature coefficient, transistor parameter tolerances and temperature dependence. Furthermore, voltage-gain stabilization, a subject for later discussion, would probably be included.

PROBLEMS

7-1 Consider the circuit of Fig. 1.

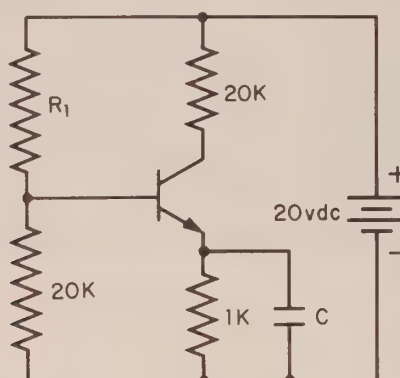


FIG. 1 Amplifier

The transistor is a silicon type with the following characteristics:

$$h_{FE} = h_{fe} = 100$$

$$h_{ie} = 4.4 \text{ k}\Omega$$

$$h_{re} = 7.3 \times 10^{-4}$$

$$h_{oe} = 24 \text{ }\mu\text{mhos}$$

$$V_{BE} = 0.6 \text{ V at } 25^\circ\text{C}$$

$$I_{co} = 0.05 \text{ }\mu\text{A (50 nA) at } 25^\circ\text{C}$$

- a. Specify a value for resistor R_1 which will establish an operating-point current I_C of approximately 0.5 mA.
 - b. What is the stability factor S_C of the amplifier?
 - c. If the reactance of C is considered negligible, what is the ac input impedance?
 - d. If capacitor C is disconnected, what is the ac input impedance?
 - e. Specify a value for C which will set the amplifier voltage gain, at a frequency of approximately 16 cps, to 3 dB greater than the dc voltage gain.
- 7-2 A circuit of the type depicted in Fig. 7-4 is to be designed using the transistor type of Prob. 7-1. The supply voltage is +20 V, and the dc load resistance is 20 k Ω .
- a. What value of base resistor R_F is required to establish a collector current of 0.5 mA?
 - b. What is the amplifier stability factor S_C ?
 - c. What would be the operating-point voltage at 75°C assuming that it is +10 V at 25°C? (Include only the effects of I_{co} and V_{BE} .)

7-3 Consider the circuit of Fig. 2.

The reactances of the coupling capacitors can be neglected, and the transistor characteristics are as indicated in Prob. 7-1.

- Select values for resistors R_1 and R_2 which will establish an emitter current of 10 mA and will also set a stability factor $(\partial I_E / \partial I_{C0})$ of approximately 10.
- What is the stage input impedance?
- What is the voltage gain e_o / e_g ?

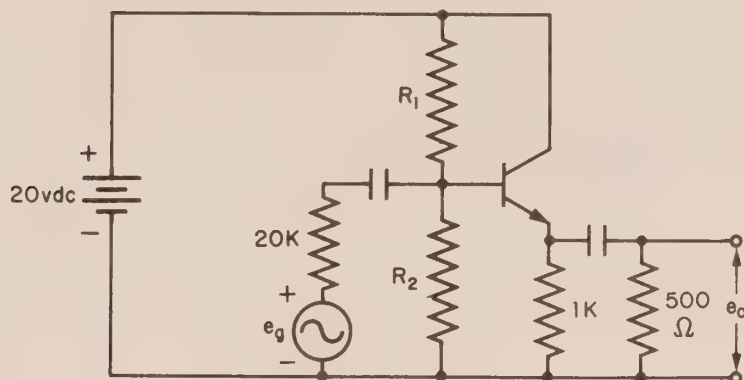


FIG. 2 Emitter Follower

7-4 Design a buffer stage to couple the output of a rate gyro-scope to a 3 K-load impedance. The rate "gyro" must operate into a constant load impedance of $10 K \pm 5\%$ ohms although the gyro output impedance is only 100Ω in magnitude.

The maximum output voltage is one volt rms, the frequency is 400 cps, and the supply voltage is 20 vdc. The stage must be ac-coupled, and the desired voltage gain is approximately one. A transistor type which has a current gain variation from unit to unit of 100 to 300 is to be used.

7-5 Consider the circuit of Fig. 3 where $e_g = E_m \cos \omega t$.

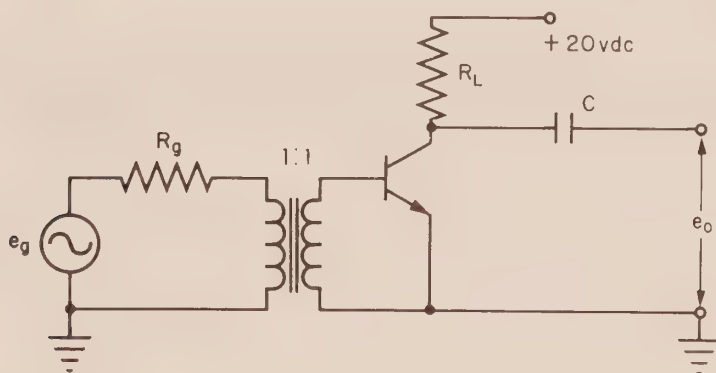


FIG. 3 Transformer-Coupled Amplifier

Assume large-signal, sinusoidal operation within the transistor ratings. Let the stage gain e_o/e_g be A and the signal frequency be ω . Assume an ideal transformer, and neglect coupling-capacitor effects.

- What is the character of the output signal?
- Write a Fourier expression for the output signal.

7-6 The circuit of Fig. 4 is to be analyzed. The transistor characteristics are as indicated in Prob. 7-1.

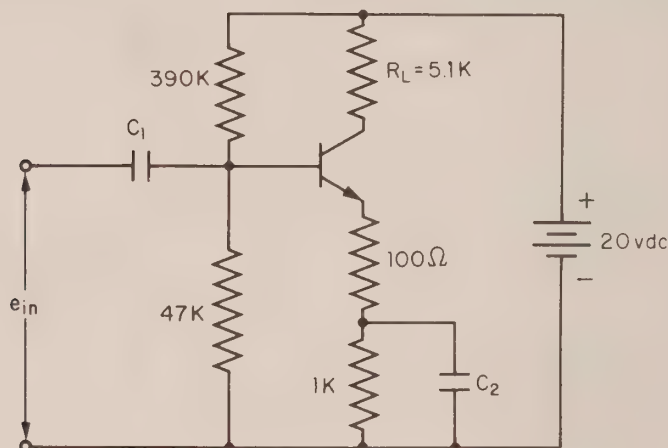


FIG. 4 AC Amplifier

- What is the dc voltage drop across resistor R_L ?
- What is the ac input impedance assuming that the capacitors are ac short circuits?
- What is the stability factor S_C ?
- What would be the dc voltage drop across resistor R_L if the transistor junction temperature were increased to 125°C ?

BIBLIOGRAPHY

Landee, Davis, and Albrecht: "Electronic Designers' Handbook," pp. 2-71 to 2-76, McGraw-Hill Book Company, New York, 1957.

AC AMPLIFIERS

8-1 RC-COUPLED CLASS A AMPLIFIERS

The design of “conventional” ac amplifiers can be considered relatively straightforward unless worst-case analysis, high reliability, or extreme stability are required. While it is possible to design a one- or two-stage amplifier for ordinary use in a few minutes, it may take a number of hours to design essentially the same circuit for production where worst-case analysis is involved. That is, in worst-case analysis, one must include the effects of power-supply variations, component tolerances, variations of transistor characteristics, temperature, age, etc. Ordinarily, the designer will select those combinations of parameter variations which cause the most adverse effects upon the circuit, and every combination will not be computed or tested because of the time and expense involved.

This chapter is intended to deal with fundamental design concepts and methods rather than with special amplifiers or amplifier problems. Fundamentals are defined here as consisting of establishment of dc operating points, calculation of input and output impedances, calculation of voltage and power gains, reliability to the extent that all components are operated within ratings, gain stabilization, and efficiency calculations which relate, also, to power-supply drain and heat generation. The circuit engineer who is proficient in only the above-defined fundamentals is perhaps the equal of the average audio-circuits engineer.

Insertion gain is a term which is used for the gain which results from the insertion of an amplifier between a generator and

its load. Consider the circuit of Fig. 8-1. The transistor characteristics are defined as follows

$$h_{fe} = 100 \text{ to } 300$$

$$h_{ie} = 4.3 \text{ k}\Omega$$

$$h_{re} = 7 \times 10^{-4}$$

$$h_{oe} = 25 \text{ }\mu\text{mhos}$$

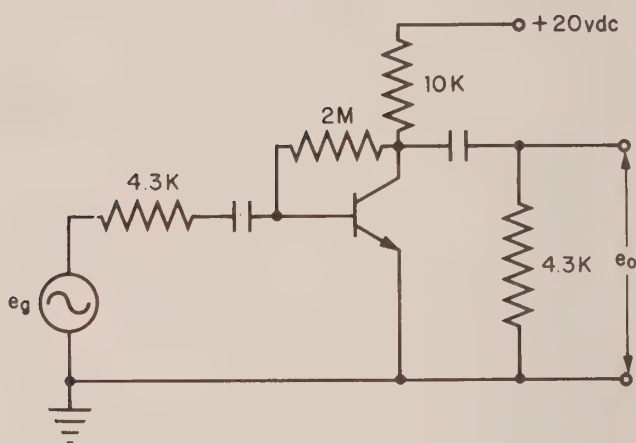


FIG. 8-1 AC Amplifier

Voltage gain (e_o/e_g) for three different values of current gain is:

h_{fe}	A_v
100	-33
200	-68
300	-104

If the 4.3K load resistor is driven directly from the voltage generator with its indicated output impedance, the voltage gain would be 1/2. Hence, the insertion voltage gain of the amplifier in the given application is -66, -136, and -208, respectively, for the three values of current gain.

One might reason that additional gain could be realized if the stage-output impedance were equal to the ac-load impedance, i.e., impedance matched. Such matching would exist if the 10 K dc load resistor were changed to 4.3 k Ω , thereby making the stage-output impedance approximately 4.3 k Ω . However, a quick calculation for voltage gain yields an answer of -24 as opposed

to -33 , indicating that a reduction in value of the dc load resistor causes a reduction in gain. Such is true because additional power is dissipated in the dc load resistor and thereby wasted. If impedance-matching were accomplished by utilizing a transformer, greater power gain would be realized because the equivalent power would not be lost in the transformer primary. Suppose the primary of a 10 K -to- 4.3 K transformer were connected in place of the ac load resistor and the secondary used to drive the load resistor. Then the voltage gain would be (for β of 100) approximately -35 as opposed to -33 , indicating an increase in gain even though the optimum impedance match is not quite obtained with the indicated turns ratio because the stage output impedance is somewhat less than $10\text{ k}\Omega$. The advantage of transformer coupling would be more evident if the impedance mismatch were worse in the original circuit.

Additional amplification would be achieved by connecting a second, identical amplifier in cascade with the amplifier of Fig. 8-1. One could anticipate a gain for the two-stage case of -33×-33 or 1,089 (for $h_{fe} = 100$). Indeed, the voltage gain of the first stage would remain at -33 because the second stage input impedance happens to equal the ac load impedance, $4.3\text{ k}\Omega$. However, the first-stage gain of -33 is the loaded gain and, therefore, the gain to the base of the second stage, and the generator impedance driving the second stage must be considered to be zero when computing the second-stage gain. The two-stage gain is:

$$\begin{aligned} A_T &= (33)(65) \\ &= 2,145 \end{aligned}$$

8-2 GAIN STABILIZATION

Voltage gain in the single-stage amplifier of Fig. 8-1 varies drastically (-33 to -104) over the indicated beta range. Gain stabilization can be achieved at some sacrifice in gain. To illustrate, suppose that a $300\text{-}\Omega$ resistor is connected in series with the emitter in Fig. 8-1. The stage voltage gains are -7.2 , -8.1 , and -9.3 for the three different values of β (100, 200, and 300), respectively. The ratio of the maximum to the minimum gain is 1.29 for the stabilized case and 3.15 for the unstabilized case, indicating that voltage gain can be stabilized against variations in transistor-current gain. See Eq. (8-0).

An expression for voltage gain with feedback (K) can be derived in terms of voltage gain without feedback (A) and a feedback fraction (β) which is the fraction of the output voltage

$$\frac{\text{Percent change in } A_v}{\text{Percent change in } B_o} = \frac{r_b + r_e + R_E + R_g}{r_b + (B_1 + 1)(r_e + R_E) + R_g} \quad (8-0)$$

where B_o is original gain, and R_E is unbypassed resistance in emitter circuit (assuming that h_{ie} varies as a function of h_{fe} , as well). B_1 is new current gain.

that is coupled back to the input. Figure 8-2 is a black-box representation of an amplifier with feedback where a fraction of the output voltage is added to the input signal.

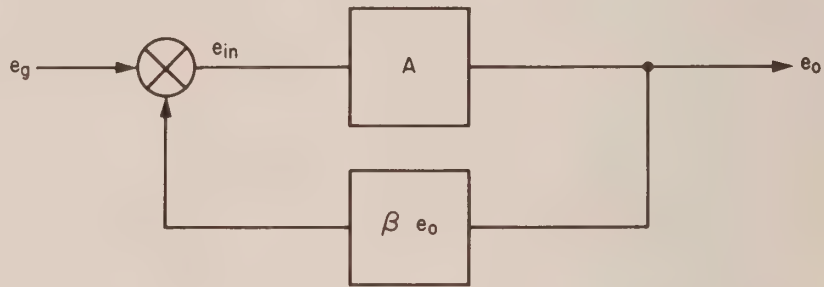


FIG. 8-2 Amplifier with Feedback

An expression for closed-loop gain is derived as follows

$$e_{in} = e_g + \beta e_o$$

$$e_g = e_{in} - \beta e_o$$

$$e_o = A e_{in}$$

$$e_g = e_{in} - A \beta e_{in}$$

$$K = \frac{e_o}{e_g}$$

$$= \frac{A e_{in}}{e_{in} - A \beta e_{in}}$$

$$K = \frac{A}{1 - A \beta} \quad (8-1)$$

Equation (8-1) defines closed-loop gain in terms of open-loop gain and the feedback fraction. Note that the amplifier is

not restricted to a single stage type, and the feedback may be either positive or negative. If phase inversion occurs between the input and output signals, then the gain A is a negative quantity, the feedback is negative, and the closed-loop gain is less in magnitude than the open-loop gain. Example 8-1 is used to illustrate the application of feedback to an amplifier.

Example 8-1

An amplifier with an open-loop gain of $-1,000$ is driven from a voltage generator with an output impedance of $10\text{ k}\Omega$. Feedback is to be added to decrease the gain (e_o/e_g) to -100 . The circuit is depicted in Fig. 8-3.

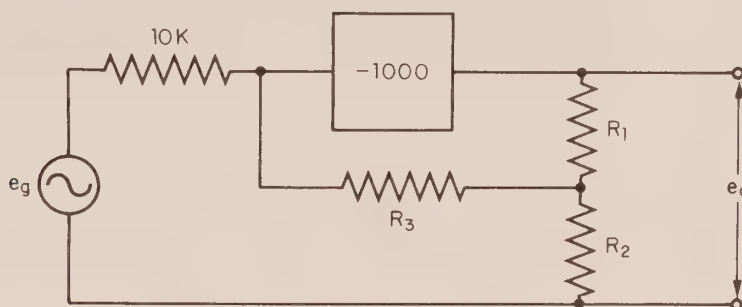


FIG. 8-3 Illustrative Example

Resistors R_1 and R_2 form a voltage divider so that a fractional value of e_o is available for feedback. In fact, the division ratio can be made equal to the feedback fraction β . The first task is to solve for β

$$\frac{A}{K} = 1 - A \beta$$

$$\frac{1,000}{100} = 1 + 1,000 \beta$$

$$\beta = 0.009$$

Setting the division ratio of R_1 and R_2 equal to β

$$\frac{R_2}{R_1 + R_2} = 0.009$$

$$R_1 = 110 R_2$$

Let the value of R_2 be 100 ohms. The value of R_1 is then 11 k Ω . The divider voltage is 0.009 e_o which should be added to the input signal on a one-to-one basis. Such is the case if the value of R_3 is set equal to the generator impedance (10 k Ω).

The actual amplifier closed-loop gain will be slightly less than -100 when the indicated resistor values are used because the divider output impedance is greater than zero ohms. However, the illustrated feedback principle is valid.

It should be noted that some generator impedance is necessary for the depicted amplifier to work as a feedback amplifier. That is, if R_g is equal to zero, the feedback voltage is shorted through the generator, and the amplifier operates open-loop.

Another aspect of interest is that the divider (R_1 and R_2) is not necessary and ordinarily is not used. A more conventional method is to use R_3 only (R_1 equals 0 and R_2 equals ∞) where the value of R_3 is calculated for the proper amount of feedback. See Sec. 9-2.

The term $1 - A\beta$ is often a useful factor. For instance, distortion is reduced by the factor $1 - A\beta$ when negative feedback is employed. Also, amplifier percentage gain variations are reduced by negative feedback, again by the factor $1 - A\beta$.

8-3 TRANSFORMER-COUPLED CLASS B AMPLIFIERS

Class B amplifiers are useful for applications which require large dynamic range with low signal distortion or better efficiency than that which can be obtained with Class A amplifiers. A typical application is in the output stage of a transistor radio where battery drain is an important factor.

Conceptually, a Class B amplifier is a two-transistor circuit in which one transistor amplifies one-half the signal waveform, and the other transistor amplifies the other half of the signal waveform. Thus, each transistor operates in the active region for half the time and in the cutoff region for half the time (assuming a symmetrical input waveform). With no input signal, battery drain is essentially zero because both transistors are biased at or near cutoff.

Crossover distortion occurs if the bias is set at cutoff, i.e., at either zero or reverse emitter-base voltage. If the emitter-base bias voltage of a transistor is zero (no forward bias), no signal amplification occurs until the signal magnitude exceeds V_{BE} . In the case of a Class B amplifier biased at cutoff, no signal amplification occurs when the signal amplitude is within the range of $\pm V_{BE}$. The specified signal is that signal which is present at the two transistor bases. Thus, a dead zone exists in which

there is no signal amplification, and the result is distortion. This problem is alleviated by applying slight forward bias to both transistors.

When designing a Class B amplifier, the designer is usually interested in such factors as power gain, dynamic range, efficiency, and sometimes distortion and frequency response. Both the common-emitter and common-collector connections are frequently used. Certain advantages of the common-collector connection can be enumerated: high input impedance, low output impedance, and simplicity of dc biasing. The required voltage gain can be realized with transformers and power gain with common-collector-connected transistors. Furthermore, thermal runaway is a lesser problem than with common-emitter amplifiers. The choice of which type of amplifier to specify is usually dictated by the particular application requirements. Figure 8-4 depicts a common-collector-connected Class B amplifier.

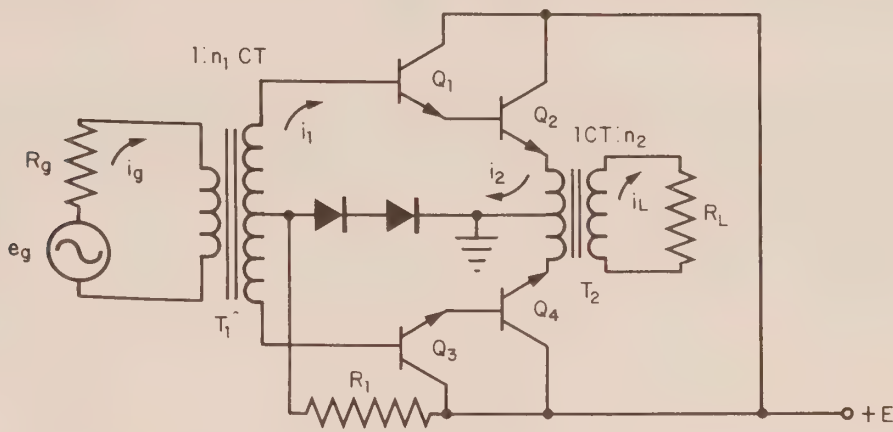


FIG. 8-4 Class B Amplifier

The two diodes and resistor R_1 in Fig. 8-4 are for the purpose of reducing crossover distortion. The dc current through the diodes should be greater in magnitude than the peak value of i_1 , the ac signal current. That is, the diodes should always be forward-biased.

Design of Class B amplifiers (or any other amplifier type, for that matter) is not always based solely upon maximum power gain. In some applications, sufficient signal power may be available, and the primary amplifier considerations may relate to voltage or impedance transformation. Nevertheless, an equation is derived here for the maximum power gain case.

The power delivered by the generator is $e_g i_g$, and the output power $e_o i_L$. Hence, power gain is:

$$A_p = \frac{e_o i_L}{e_g i_g}$$

An equation for i_L in terms of i_g is required:

$$i_L = \frac{i_2}{2n_2}$$

$$i_2 = B_1 B_2 i_1$$

$$i_1 = \frac{2 i_g}{n_1}$$

Solving for i_L :

$$i_L = \frac{B_1 B_2 i_g}{n_1 n_2}$$

where B_1 and B_2 are the current gains of transistors Q_1 and Q_2 , respectively. It is assumed that transistors Q_1 and Q_3 are identical and that transistors Q_2 and Q_4 are identical

$$\frac{i_L}{i_g} = \frac{B_1 B_2}{n_1 n_2}$$

$$\frac{e_o}{e_g} = A_v$$

Hence, power gain is given by Eq. (8-2)

$$A_p = \frac{A_v B_1 B_2}{n_1 n_2} \quad (8-2)$$

The total number of secondary turns divided by the total number of primary turns of transformers T_1 and T_2 is defined as n_1 and n_2 , respectively.

If the transformers are ideal, the emitter-follower voltage gain is one, and R_g is zero, then the stage voltage gain is simply the product of the transformer turns ratios, and Eq. (8-2) reduces to Eq. (8-3)

$$A_p \cong B_1 B_2 \quad (8-3)$$

For the maximum power gain case, the amplifier input impedance, as referenced to the primary of transformer T_1 , must

be equal to the generator impedance R_g . Input impedance is calculated next. The reflected impedance at the emitter of Q_2 is $R_L/4n_2^2$, and one could use Eq. (5-36) to find the impedance at the base of Q_1 . However, the emitter follower input impedance is approximately $B_1 B_2 R_L/4n_2^2$. This impedance is transferred to the primary of T_1 , and the stage input impedance is then given by Eq. 8-4:

$$R_{in} \cong \frac{B_1 B_2 R_L}{(n_1 n_2)^2} \text{ ohms} \quad (8-4)$$

For maximum power transfer, R_g must equal R_{in} and Eq. (8-5) results

$$\frac{(n_1 n_2)^2}{B_1 B_2} = \frac{R_L}{R_g} \quad (8-5)$$

The other controlling factor for maximum power transfer is that the stage output impedance must equal the load impedance. Equation (5-39) defines emitter-follower output impedance, but the approximation of R_g divided by β is used here for output impedance. With this assumption, output impedance is given by Eq. (8-6)

$$R_o \cong \frac{R_g (n_1 n_2)^2}{B_1 B_2} \text{ ohms} \quad (8-6)$$

Since R_o must equal R_L , Eq. (8-6) reduces back to Eq. (8-5). Hence, the relationship of R_L to R_g is defined by Eq. (8-5) in terms of the transformer turns ratios and the transistor current gains for the maximum-power-transfer case.

In the customary situation, the designer is confronted with fixed generator and load impedances; so the variables in Eq. (8-5) are transistor current gains and transformer turns ratios. Transistors are then selected for maximum beta consistent with other electrical parameters and price. It would appear a simple matter to select transformer types with appropriate power and frequency ratings and turns ratios as calculated from Eq. (8-5). However, transistor voltage ratings must be observed, and this limits the choice of turns ratios.

If transistor Q_2 is driven to saturation by the input signal, the peak voltage at the emitter of Q_2 equals the supply voltage ($+E$). At this instant, because of transformer action, the voltage

at the emitter of Q_4 is the negative of the supply voltage ($-E$). Since the collector is at $+E$ and the emitter at $-E$, the maximum collector-emitter voltage is twice the supply voltage if the amplifier is driven to saturation. Such is true for all four transistors in Fig. 8-4.

8-4 EFFICIENCY

If efficient electronic circuitry is of concern, it is usually because primary power is limited, and/or heat generation is a problem. Satellite applications are power limited and require efficient equipment, particularly in the power conversion circuits.

It is easily demonstrated that the efficiency of Class A amplifiers is 50 percent since half the supply voltage is, on a dc basis, across the transistor and half across the load impedance. Class B amplifiers can, however, be more than 50 percent efficient.

Efficiency is equal to output power divided by input power, or, alternately, output power divided by the sum of output power and losses. In the circuit of Fig. 8-4, output power is equal to the rms emitter voltage of transistor Q_2 (or Q_4) multiplied by the rms value of i_2 (assuming an ideal output transformer). In terms of peak values, the output power, for sinusoidal operation, is

$$P_o = \frac{e_p i_2}{2}$$

where e_p equals peak emitter voltage, and i_2 equals peak emitter current.

The line current waveform is a full-wave rectified sinusoid with an average value of $2/\pi$ times the peak current. Hence, the input power is

$$P_{in} = \frac{2E i_2}{\pi}$$

Efficiency is equal to power out over power in which, for a Class B amplifier with resistive load, is given by Eq. (8-7)

$$\eta = \frac{\pi e_p}{4E} \quad (8-7)$$

where e_p equals peak emitter voltage, and E equals the dc supply voltage.

Thus, maximum Class B efficiency occurs when e_p equals E which is when the output transistors are driven just to saturation by the peaks of the input signal. Given ideal transformers, maximum Class B efficiency is approximately 78.5 percent.

If the output load impedance is reactive, a phase angle exists between e_p and i_2 , and output power is decreased by the cosine of the phase angle. Input power, however, varies only with impedance magnitude and not with impedance phase angle. Such is true because input power is a function of dc quantities, wherein no phase angle is involved. Thus, the general expression for sinusoidal Class B efficiency is given by Eq. (8-8)

$$\eta = \frac{\pi e_p \cos \theta}{4E} \quad (8-8)$$

where e_p equals peak emitter voltage, E equals the dc supply voltage, and θ equals the phase angle between output current and voltage.

In the event that a common-emitter-connected amplifier is under consideration, e_p in Eq. (8-8) is redefined as the peak voltage from primary to center tap of the output transformer.

It is emphasized that, for completely reactive loads, output power in watts is zero, and all the input power is dissipated in the transistors. Therefore, amplifier-output power rating is better specified in terms of volt-amperes rather than watts if the load is complex.

8-5 EMITTER FOLLOWERS

Emitter followers are often used in large signal operation as buffers or drivers. A common mistake is to apply small-signal formulas to the large-signal case, particularly with regard to output impedance. Consider the circuit of Fig. 8-5.

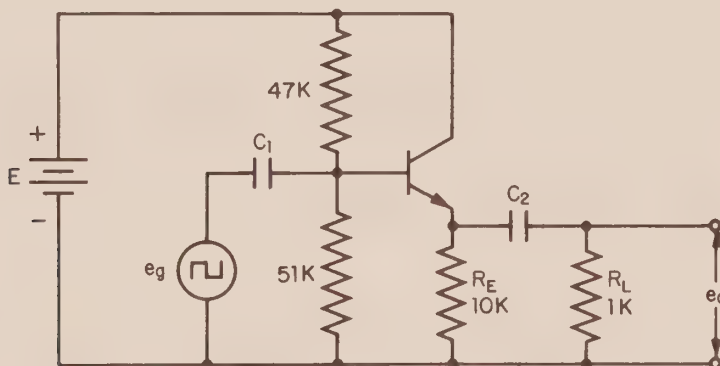


FIG. 8-5 Emitter Follower

The small-signal output impedance of the transistor in Fig. 8-5 is given as 40 ohms, and it would appear that there would be no difficulty in driving a 1 K load impedance. Such is not the case, however, for large-signal operation. The output waveform, for sinusoidal inputs, is distorted with the bottoms of the sine wave flattened or clipped off. The reason is that the transistor is driven into cutoff by the negative signal peaks. This is true even though the input signal swing is supposedly within the amplifier's dynamic range. Such can be demonstrated by disconnecting the 1 K ac load resistor whereupon clipping ceases.

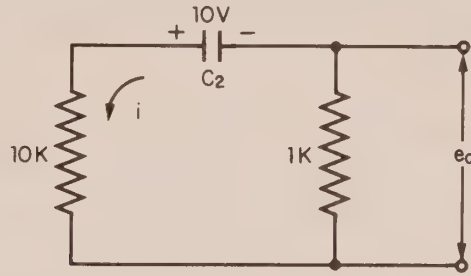
Current conduction in an emitter follower or cathode follower is unidirectional. Magnitude variations, i.e., more or less current, are obtained by modulating the dc-operating-point current, but dc current reversal does not occur. That is, conventional current does not conduct from cathode to plate or from emitter to collector (in an NPN transistor). Either device merely goes into the high impedance cutoff state when ac requirements are for negative current (current back into the cathode or emitter). Thus, it can be visualized how a cathode follower can be designed to charge capacitance quite rapidly but yet be incapable of discharging the same capacitance. The capacitance is charged from current through the tube, but the discharge path is through the cathode dc load resistor. Any current from the tube is in a direction to charge, not discharge, the capacitance. Hence, the shortest discharge time occurs when the tube or transistor is driven to cutoff.

A generalized formula can be derived from the specific circuit of Fig. 8-5. For purposes of illustration, a square-wave input signal with a peak amplitude of e_p is assumed. Let the supply voltage E be 20 V and the dc-operating-point current I_E be one mA. When the input signal switches to $+e_p$, the emitter voltage also switches to $+e_p$ since voltage gain is essentially one. The output signal also is $+e_p$ assuming that $C_2 R_L$ is very large, and the output current is e_p/R_L .

When the input signal switches to $-e_p$, the transistor is driven toward cutoff, and it is assumed that it is driven into the cutoff state. The circuit then reduces to resistors R_E and R_L and capacitor C_2 . The charge contained in C_2 is of interest. Let t equal the half-period of the input signal. Before an input signal was applied, the voltage across C_2 was the dc-operating-point voltage, 10 V. At the instant that the input signal switches from $+e_p$ to $-e_p$, the capacitor voltage is

$$V_{C_2} = 10 + \frac{(e_p)(t)}{C_2 R_L} \text{ volts}$$

However, if $C_2 R_L$ is much greater than t , then the capacitor voltage is simply 10 V. Thus, the equivalent circuit is:



Again assuming that C_2 is very large, the output voltage is:

$$\begin{aligned} e_o &= (i)(1K) \\ &= \left(\frac{-10}{11K} \right) (1K) \\ &= -1 \text{ volt} \end{aligned}$$

It is apparent that the output signal is limited in the negative direction to a magnitude of approximately 1 volt, whereas the positive limit is almost 10 volts. It is also evident that the emitter voltage remains clamped at approximately +9 volts while the base is at the voltage $(10 - e_p)$, which verifies that the base-emitter junction is reverse-biased and the transistor cutoff if the magnitude of e_p is greater than one volt.

Clearly, then, an equation can be written for the maximum peak output voltage (negative peak for an NPN transistor and positive peak for a PNP transistor) in terms of the dc-operating-point voltage and resistors R_E and R_L . See Eq. (8-9).

$$e_p = \frac{(R_L)(E_o)}{R_E + R_L} \text{ volts} \quad (8-9)$$

where E_o is the dc-operating-point voltage, R_E is the emitter resistor, and R_L is the ac load resistor.

Equation (8-9) indicates the maximum value of the negative peak (for an NPN transistor) and should not be used to find the positive peak.

The dynamic range or clipping problem is apparent also if one draws the ac load line on the static collector characteristic curves. As a matter of practice, however, engineers do not

draw load lines on transistor curves with the same frequency as in vacuum tube problems.

Large signal operation can, in fact, cause a shift in the dc operating point, but this effect is not considered here.

8-6 DESIGN EXAMPLE

The output stage of a 400-cps sinusoidal static inverter is to be designed. Maximum rated output is 100 VA, and the line voltage is 24 to 31 vdc. The load phase angle may be anywhere from 0.7 leading to 0.7 lagging, and the desired output amplitude is 26 vrms.

A circuit of the type depicted in Fig. 8-4 is considered appropriate, and transistors are selected with the following characteristics:

$$Q_1, Q_3 \quad h_{FE} = 100$$

$$r_{sat} = 5 \Omega$$

$$P_c = 10 \text{ W}$$

$$Q_2, Q_4 \quad h_{FE} = 50$$

$$r_{sat} = 0.05 \Omega$$

$$P_c = 100 \text{ W}$$

The transformers are assumed ideal for this example except for dc resistance in the primary of the output transformer, which is specified by the Circuit Designer to be 0.1Ω maximum across the whole primary. Turns ratio of T_2 is the first parameter to be calculated. Secondary current of T_2 is

$$i_s = \frac{P_o}{e_o}$$

$$= \frac{100}{26}$$

$$= 3.85 \text{ A rms}$$

$$= 5.44 \text{ A peak}$$

The maximum allowable peak voltage at the emitter of Q_2 (or Q_4) is

$$e_p = 24 - (5.44 n) \left(\frac{0.1}{2} + \frac{5}{50} \right) \text{ volts}$$

Note that Q_1 saturates before Q_2 and that only half the primary dc resistance is involved at any one time. Here, n is the turns ratio from one-half the primary to the secondary.

The magnitude of the voltage which is transformed from one-half the primary to the secondary is as follows:

$$e_s = n \left[e_p - (5.44 n) \left(\frac{0.1}{2} \right) \right]$$

That is, the secondary voltage is less than $n e_p$ because of transformer regulation. However, the error is small and can be neglected, especially since the final turns ratio must be rechecked anyway. Therefore, let e_p equal e_s/n .

$$\begin{aligned} e_p &= \frac{e_s}{n} \\ &= \frac{26\sqrt{2}}{n} \\ &= \frac{36.7}{n} \text{ volts} \end{aligned}$$

Substituting into the primary equation:

$$\frac{36.7}{n} = 24 - (5.44 n) \left(\frac{0.1}{2} + \frac{5}{50} \right)$$

$$n \cong 1.65$$

This turns ratio is that from one-half the primary to the secondary. Thus, the transformer turns ratio can be written as $2CT:1.65$. With the indicated turns ratio, the peak primary voltage would be approximately 22.5 volts, which means that the transistors are driven near saturation when the line voltage is at 24 vdc. Some design margin is desirable, and the tendency

is to design for a peak primary voltage much less than the maximum allowable. A constraint is imposed on the lower limit, however, by efficiency and power dissipation, particularly when the line voltage is at 31 vdc. Furthermore, the greater the step-up ratio from primary to secondary the greater the primary current (transistor current) which increases the difficulty in driving the input transformer.

Obviously, a compromise is in order, and the peak primary-to-center-tap voltage is chosen to be 20 volts which means a turns ratio for T_2 of $2CT:1.84$. It should be recognized that the primary voltage exceeds 20 volts at full output, assuming constant output voltage, because of transformer regulation. This would be a known quantity, however, and of the order of 5 percent. Thus, for full-load output voltage of 26 vrms, the half-primary peak voltage would be approximately 21 volts.

The full-load primary current i_2 can now be calculated and thereafter the current i_1 , as well

$$\begin{aligned} i_2 &= (5.44)(1.84) \\ &= 10 \text{ A peak} \end{aligned}$$

The current i_1 is equal to i_2 divided by the product of the transistor β 's.

$$\begin{aligned} i_1 &= \frac{10}{5,000} \\ &= 2 \text{ mA peak} \end{aligned}$$

The current through resistor R_1 must exceed 2 mA. Let the value of R_1 be 7.5 k Ω . The resistor current is then not excessive, and the diodes are always forward biased.

An optimum turns ratio for T_1 cannot be calculated because the generator impedance and allowable dynamic range at the primary of T_1 are not known. In all probability, these factors would be known. Let R_g be equal to 1 k Ω . Then Eq. (8-5) can be used to solve for the T_1 turns ratio.

$$n_1 n_2 = \left(\frac{B_1 B_2 R_L}{R_g} \right)^{1/2}$$

The minimum load resistance is:

$$\begin{aligned} R_L &= \frac{(26)^2}{100} \\ &= 6.75 \Omega \end{aligned}$$

Then n_1 is as follows:

$$n_1 = \frac{\sqrt{33.75}}{1.84/2}$$

$$= 6.3$$

Hence, the turns ratio of T_1 is 1:6.3CT, and the peak primary voltage is less than 7 volts or 14 volts peak to peak. It is assumed that this is within the dynamic range of the T_1 driver stage.

Worst-case efficiency for the Class B amplifier must be calculated in order to determine power dissipation in the transistors. Equation (8-8) is applicable

$$\eta = \frac{(78.5)(0.7)(21)}{31}$$

$$= 37\%$$

The input power is:

$$P_{in} = \frac{100}{0.37}$$

$$= 270 \text{ W}$$

Power dissipated in the transistors is power in minus power out or 170 W which is equally divided between each half of the Class B power transistors. Thus, transistors Q_2 and Q_4 are each dissipating approximately 85 W when driving a load impedance of 6.75 Ω at a power factor of 0.7 and at the highest line voltage (31 vdc). Transistors Q_1 and Q_3 are dissipating 85 divided by 50 or 1.7 W, each. All transistors are operating within the specified ratings.

PROBLEMS

- 8-1 What is the open-loop gain of an amplifier if the closed-loop gain is -50 , the feedback is negative, and the feedback fraction is 0.01 ?
- 8-2 In the circuit of Fig. 8-4, all transistor current gains are 100 and R_L is $10\ \Omega$ resistive.
- What is the input impedance at the primary of T_1 ? Assume that the voltage generator e_g is disconnected ($R_g = \infty$).
 - What is the power gain in dB if R_g is zero ohms and the transformers are ideal?
 - If the line voltage is 28 vdc and the peak sinusoidal signal at the emitter of Q_2 is 20 V , what is the efficiency? Again assume ideal transformers.
 - What is the efficiency if R_L is equal to $j10\ \Omega$?
- 8-3 Consider the circuit of Fig. 1.

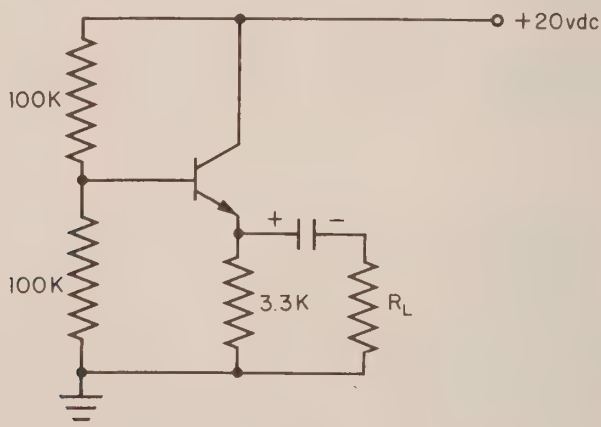


FIG. 1 Emitter Follower

If the peak-to-peak signal at the base of the transistor is 5 volts , what is the minimum value that R_L can be before signal clipping occurs? The transistor is a silicon type with a current gain of 100 . Assume that the emitter-follower voltage gain is 1 in the linear region. (The dc operating point must be determined, however.)

- 8-4
- What is the input impedance of the circuit depicted in Fig. 2? Assume ideal rectifiers and transformer.
 - What would be the input impedance if the rectifiers were short circuited?
- 8-5 Consider the circuit of Fig. 3, and assume small-signal operation.

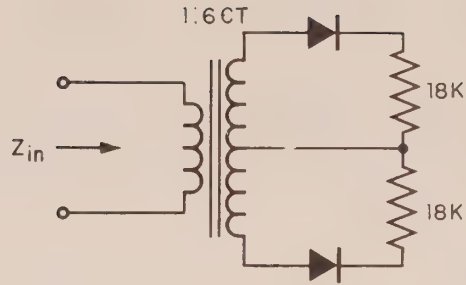


FIG. 2 Transformer Problem

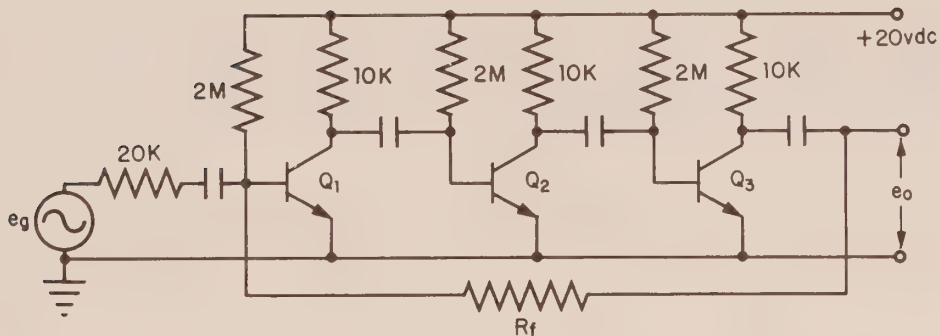


FIG. 3 Feedback Amplifier

At signal frequencies, the coupling capacitors are ac short circuits. The three transistors are identical and have the following characteristics:

$$h_{fe} = h_{FE} = 100$$

$$h_{ie} = 5 \text{ k} \Omega$$

$$h_{re} = 8 \times 10^{-4}$$

$$h_{oe} = 25 \text{ } \mu\text{mhos}$$

- If R_f is infinite, what is the voltage gain e_o/e_g ?
- If R_f is equal to $2 \text{ M}\Omega$, what is the gain?

8-6 The characteristics of the transistor in Fig. 4 are as defined in Prob. 8-5.

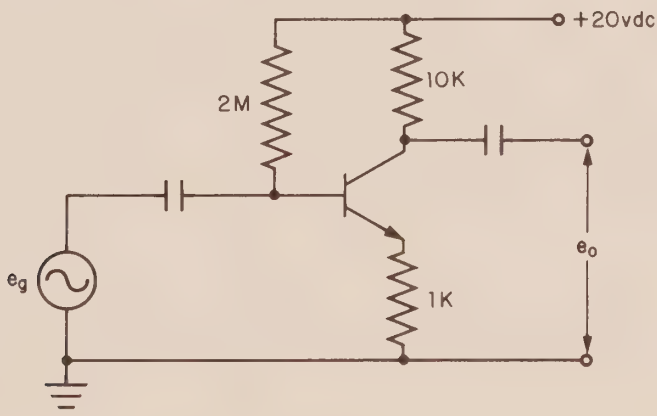


FIG. 4 Transistor Amplifier

At signal frequencies, the coupling capacitors are ac short circuits.

- a. Compute the voltage gain e_o/e_g by using the feedback formula, Eq. (8-1). (The open-loop gain is found by assuming that the 1 K-emitter resistor is short circuited.)
 - b. Compute the aforementioned gain by using Eqs. (5-40) and (5-44).
- 8-7 How many transistors are required to implement an amplifier with a voltage gain (e_o/e_g) of 400? Note that there is no phase inversion between input and output signals.
- 8-8 Complete the design of the circuit depicted in Fig. 5 so that the gain is

$$K = e_o/e_g$$

$$= 10 \angle 135^\circ$$

The transistor characteristics are defined in Prob. 8-5.

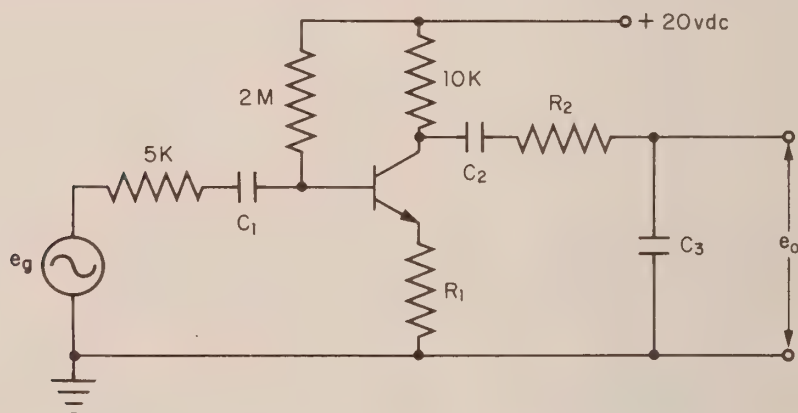


FIG. 5 Amplifier Problem

Capacitors C_1 and C_2 are to be considered ac short circuits at the signal frequency which is 1,000 cps, and the input signal is sinusoidal.

DC AMPLIFIERS

9-1 DIFFERENTIAL AMPLIFIERS

Direct-coupled amplifiers can be a vast subject if all variations and aspects are considered. However, basic equations and techniques are usually sufficient for ordinary dc-amplifier applications. Difficult or unusual problems are likely to be referred to a dc-amplifier specialist or the part purchased from various companies which manufacture such items.

Differential or difference amplifiers are useful for amplifying the difference between two signals, either ac or dc. Such amplifiers possess two input points, one of which may be grounded, and one or two output points depending upon whether or not the output is single- or double-ended. An obvious advantage of differential amplifiers is that they amplify only the difference between two input signals, and the amplification of common signals is slight. *Common-mode rejection* is a term which relates the amplification of equal signals to amplification of differential signals. If the common-mode rejection of an amplifier is high, the amplification of common signals is relatively low. Figure 9-1 depicts a differential or difference amplifier (dc-biasing circuits not shown).

In order that the common-mode rejection and differential gain be high, the current I_E should be constant, which means that resistor R_E should be quite large. That is, a constant-current generator connected in place of R_E would be ideal. In fact, R_E is often replaced with a common-collector-connected transistor to ensure that I_E is constant. This is possible since the collector current of an emitter follower is essentially independent of

collector-to-emitter voltage if the base is connected to a fixed voltage.

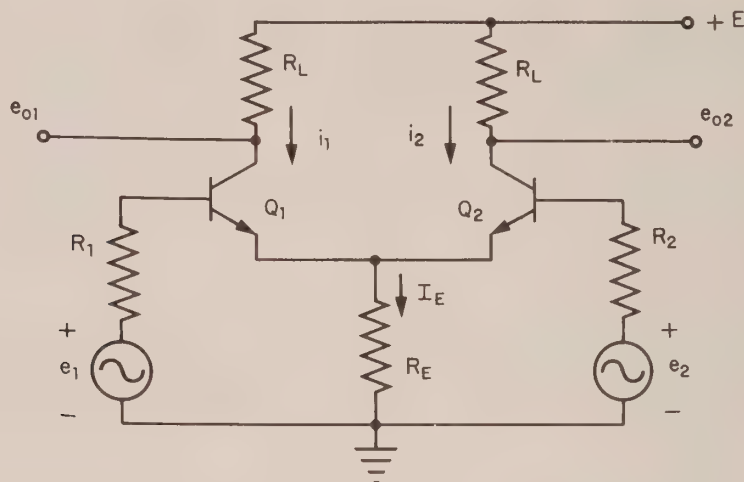


FIG. 9-1 Differential Amplifier

Voltage gain for the circuit of Fig. 9-1 is calculated with the assumption that I_E is constant and equal to the sum of i_1 and i_2 . The desired result could be obtained from the application of Eqs. (5-40) and (5-44) if the impedance from emitter to ground were known. Let the voltage e_2 be 0. Then the single-ended voltage gain is (from Eq. 5-44)

$$A_v \cong \frac{-h_{fe}}{(R_{in} + R_1)(Y_L + h_{oe})}$$

Although the value of R_E is considered to be quite large, the impedance from Q_1 emitter to ground is not necessarily large since Q_2 is operating in the linear region and presents a load to transistor Q_1 . The loading of Q_2 can be considered from two standpoints: common-collector output impedance or common-base input impedance. In either case, the loading impedance R at the emitter of Q_1 is approximately:

$$R \cong h_{ib} + \frac{R_2}{h_{fe} + 1}$$

$$(h_{fe} + 1)R = h_{ie} + R_2$$

Equation (5-40) is then used to find the Q_1 input impedance:

$$\begin{aligned} R_{in} &= h_{ie} + h_{ie} + R_2 \\ &= 2h_{ie} + R_2 \end{aligned}$$

Single-ended voltage gain (collector to ground) is defined by Eq. (9-1):

$$A_v \cong \frac{-h_{fe}}{(2h_{ie} + R_1 + R_2)(Y_L + h_{oe})} \quad (9-1)$$

Double-ended voltage gain (collector to collector) is twice the single-ended gain if the two load impedances are equal.

Voltage gain as expressed by Eq. (9-1) is e_{o1}/e_1 where e_2 is 0, or, alternately, it is e_{o2}/e_2 where e_1 is 0. It is not necessary to modify Eq. (9-1) when both e_1 and e_2 are finite; it is only necessary to redefine A_v

$$\begin{aligned} A_v &= \frac{e_{o1}}{e_1 - e_2} \\ &= \frac{e_{o2}}{e_2 - e_1} \end{aligned}$$

Note that e_{o1} equals $-e_{o2}$ (phase inverted) if both collector load impedances are equal.

Example 9-1

Certain regulated voltages are required in a particular system where the only input voltage is 27 ± 3 vdc. One required voltage level is +15 vdc which must be regulated to within ± 1 percent. The problem is to design a 15-V regulator which operates from the line voltage, 27 ± 3 V, and which is capable of driving a 100 mA load. Regulation characteristics are to be examined as a function of variations in steady-state values of line voltage and load current. (Room temperature operation is specified.)

The amplifier which is depicted in Fig. 9-2 is proposed to satisfy the design assignment. Some arithmetical operations are necessary to finish the design and to prove that regulation is satisfactory. Transistors are specified with the following characteristics:

$$\begin{aligned} Q_1: \quad h_{FE} &= 50 \\ h_{ie} &= 1.5 \text{ k}\Omega \end{aligned}$$

Q_2, Q_3, Q_4 : Conditions: $I_c = 1 \text{ mA}$, $V_{CE} = 5 \text{ V}$

$$h_{FE} = 100$$

$$h_{ie} = 5 \text{ k}\Omega$$

$$h_{oe} = 25 \text{ }\mu\text{mhos}$$

The minimum magnitude of Q_2 base current is

$$\begin{aligned}(I_{B2})_{\min} &= \frac{100}{(50)(100)} \\ &= 20 \text{ }\mu\text{A}\end{aligned}$$

If transistors Q_1 and Q_2 are silicon types, the voltage at the base of Q_2 is approximately 15 plus 1.2 or 16.2 volts.

$$\begin{aligned}(R_1)_{\max} &= \frac{7.8 \text{ V}}{20 \text{ }\mu\text{A}} \\ &= 390 \text{ k}\Omega\end{aligned}$$

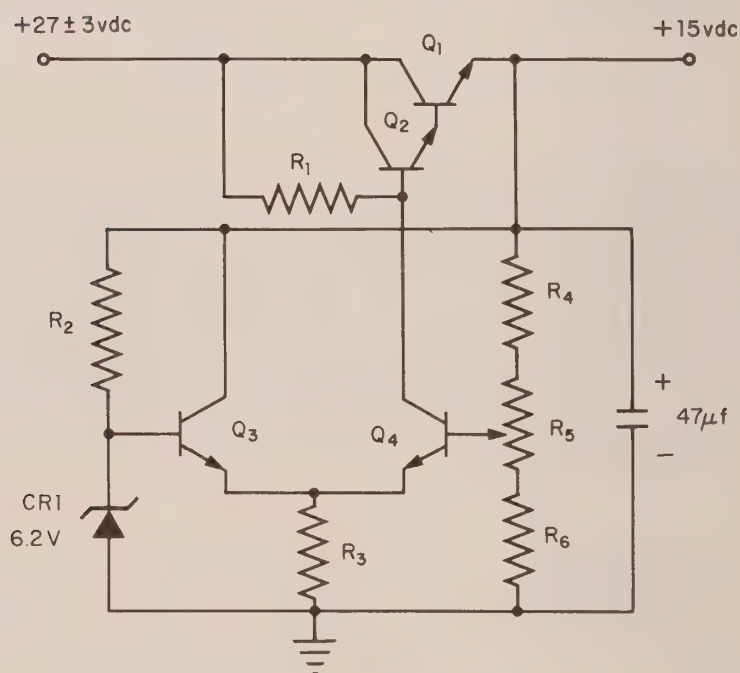


FIG. 9-2 DC Regulator

However, transistors Q_3 and Q_4 must be operated at currents near 1 mA if the associated current gains are to be high.

Resistor R_1 must be smaller in magnitude to reduce leakage current effects, as well. Let the collector current of transistor Q_4 (and also Q_3) be approximately 0.5 mA. The appropriate value for resistor R_1 is, then, 15 k Ω .

The voltage at the emitter of Q_3 is 6.2 minus 0.6 or 5.6 V. Since under balanced conditions the collector currents of Q_3 and Q_4 are equal, the current through R_3 is 1 mA which requires that R_3 be 5.6 k Ω .

The temperature-voltage coefficient of zener diode CR_1 is optimized if the diode current is 5 mA. Hence, resistor R_2 is 1.8 k Ω in value.

A divider current (through R_4 , R_5 , and R_6) equal to one percent of the maximum output current is not considered excessive. One percent of the output current is 1 mA which is much greater than the Q_4 base current. If the divider current is made quite low, loop-voltage gain will be diminished, and amplifier drift will be increased. In fact, for optimum stability, the base-to-ground impedance at the base of Q_4 should equal the like impedance at the base of Q_3 , which is that of a conducting Zener diode and which is less than 100 Ω .

However, let the sum of R_4 , R_5 , and R_6 be 15 k Ω , and let R_5 be a 1-K potentiometer. The values of the other resistors are easily calculated since the base voltage of Q_4 must also be approximately 6.2 V.

$$R_6 = 5.6 \text{ k}\Omega$$

$$R_4 = 8.2 \text{ k}\Omega$$

Loop gain is calculated by applying Eq. (9-1) and assuming that the load impedance for Q_4 is 15 k Ω

$$Q_3 \text{ generator impedance} \cong 100 \Omega$$

$$Q_4 \text{ generator impedance} \cong 3.6 \text{ k}\Omega$$

Differential amplifier voltage gain:

$$\begin{aligned} |A_v| &= \frac{100}{(10 \text{ K} + 100 + 3.6 \text{ K})(1/15 \text{ K} + 25 \times 10^{-6})} \\ &= 84 \end{aligned}$$

Divider gain factor

$$\begin{aligned} K &= \frac{6.2}{15} \\ &= 0.415 \end{aligned}$$

Gain of Q_1, Q_2 at $I_o = 100$ mA:

For $Q_2, A_v \cong 0.97$

For Q_1 from Eq. (5-37);

$$A_v = \frac{50}{(1500 + 200)(1/150) + 50}$$

$$= 0.81$$

Compound emitter-follower gain = $(0.97)(0.81)$

$$= 0.785$$

Loop gain = $(84)(0.415)(0.785)$

$$= 27.5$$

In the open-loop case at maximum output current, a 3-V line change would result in a 2.36-V (0.785×3) output change. In the closed-loop case, the output change would be approximately 86 mV ($2.36/27.5$), or a change of 0.57 percent, which is within the specification limit.

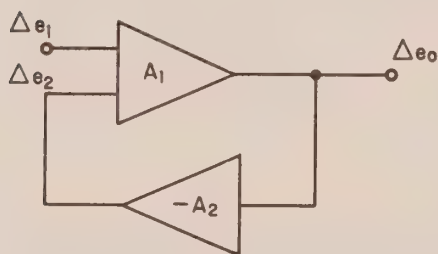


FIG. 9-3 Feedback Amplifier

A better concept of the function of the feedback loop can be realized by considering Fig. 9-3.

Amplifier A_1 is the emitter follower which has a gain of 0.785, and amplifier A_2 is the differential amplifier and divider combination which has a gain of 84×0.415 . One-for-one summing at the base of Q_2 is assumed, and Δe_1 is the line voltage change. The analysis

continues:

$$\begin{aligned} \Delta e_o &= (\Delta e_1 + \Delta e_2) A_1 \\ &= (\Delta e_1 - A_2 \Delta e_o) A_1 \end{aligned}$$

Solving for Δe_o as a function of Δe_1 :

$$\begin{aligned} \Delta e_o &= \frac{(A_1)(\Delta e_1)}{1 + A_1 A_2} \\ &= \frac{(A_1)(\Delta e_1)}{1 + \text{loop gain}} \end{aligned}$$

In other words, one would be justified in dividing the open-loop output voltage change by 28.5 rather than by 27.5.

Output impedance of the Q_1 and Q_2 combination is computed from Eq. (5-39) to be approximately 35 ohms. Thus, the open-loop regulation from no-load to full-load is as follows:

$$\begin{aligned}\Delta e_o &= 15 - I_L R_o \\ &= 15 - (0.1)(35)\end{aligned}$$

$$\Delta e_o = 3.5 \text{ volts}$$

Closed-loop voltage change is:

$$\begin{aligned}\Delta e_o &= \frac{3.5}{27.5} \\ &= 127 \text{ mV}\end{aligned}$$

The closed-loop output change from no-load to full-load is 0.85 percent.

If the output voltage is adjusted to 15 V at an output current of 50 mA, then variations of line and load would result in output variations within the specified limit of ± 1 percent.

9-2 OPERATIONAL AMPLIFIERS

An operational amplifier is composed of a specially designed dc amplifier and input and feedback impedances. Such amplifiers are used to perform various mathematical operations such as addition, subtraction, multiplication, integration, etc. Analog computers, for instance, make use of many operational amplifiers in solving a given analog problem. The solution is not, however, exact in the sense of unlimited significant figures. That is, operational amplifiers are analog as opposed to digital or discrete devices, and analog computing accuracies in the range of 0.1 to 1 percent are common. The slide rule is a good example of an analog computing device.

Desirable characteristics for an operational amplifier include low drift, low offset (zero output for zero input), high open-loop gain, and controlled phase shift and frequency response. Figure 9-4 is the conventional representation for an operational amplifier.

An object in employing an operational amplifier is to generate a transfer function e_o/e_{in} which is dependent only on the

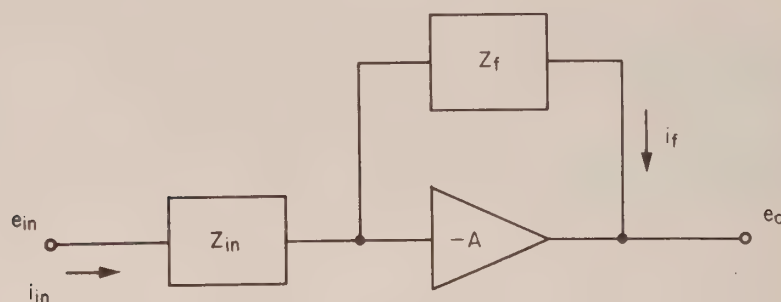


FIG. 9-4 Operational Amplifier

input and feedback impedances and not on the amplifier. If the amplifier is ideal and the open-loop gain A is infinite, such is the case. One can visualize this result with the following logic. The voltage at the junction of Z_{in} and Z_f must be zero for the amplifier to operate linearly since any finite input voltage will result in infinite output voltage, limited, of course, by amplifier saturation. Amplifier input current is zero; hence, i_{in} equals i_f , e_o equals $-i_f Z_f$, and e_{in} equals $i_{in} Z_{in}$. Equation (9-2) is, then, evident for the ideal amplifier

$$\frac{e_o}{e_{in}} = \frac{-Z_f}{Z_{in}} \quad (9-2)$$

If the amplifier open-loop gain (A) is finite, the transfer function can be found from Eq. (9-3):

$$\frac{e_o}{e_{in}} = \frac{-Z_f}{(Z_{in} + Z_f)/A + Z_{in}} \quad (9-3)$$

It should be noted that neither the input nor feedback impedance need be composed of a single component. For instance, an adder may be constructed by connecting two or more resistors to the input and using a single feedback impedance. Ideally, the voltage gain for each input signal is as indicated by Eq. (9-2) where Z_{in} equals the value of the particular input resistor. To illustrate, consider the ideal amplifier of Fig. 9-5.

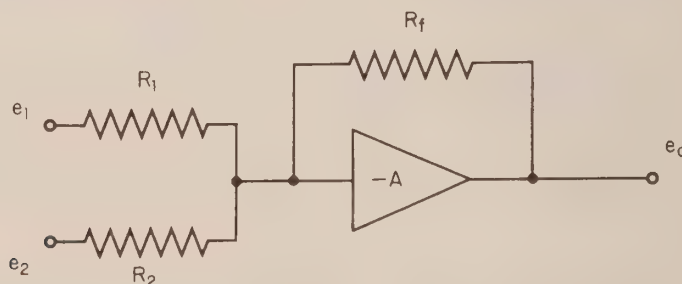


FIG. 9-5 Operational Adder

The output signal as a function of the input signals is:

$$e_o = -R_f \left(\frac{e_1}{R_1} + \frac{e_2}{R_2} \right) \text{ volts}$$

Considerable flexibility is possible with the adder of Fig. 9-5 since one can choose values for R_1 , R_2 , and R_f over a wide range. If, for instance, all resistors are made equal, the output voltage is the phase-inverted sum of the two input voltages. Furthermore, one is not limited to summing only two signals; practical limits depend upon the particular case, but one might sum as many as 10 or more signals.

A wide variety of transfer functions can be realized by choosing the proper feedback and input impedances. For instance, an integrator could be devised by replacing R_f in Fig. 9-5 with a capacitor. Equation (9-4) describes such a case where the voltage across the capacitor is zero at time equals zero

$$e_o = -\frac{1}{C} \int_0^t \left(\frac{e_1}{R_1} + \frac{e_2}{R_2} \right) dt \quad (9-4)$$

9-3 VIDEO AMPLIFIERS

Video amplifiers are used to amplify wide-band signals where the required frequency response may be from dc to several megacycles per second. Such amplifiers are frequently used to amplify pulse trains in television or radar receivers.

Only the more rudimentary aspects of video amplifiers are considered here since the design of anything other than a simple amplifier can be quite complex and require considerable rigor. However, if one is not designing for high-volume, low-cost production, basic tenets are sufficient.

In the design of video amplifiers, the first questions that must be answered are: How many stages are necessary to satisfy the gain requirements, and what bandwidth is required? The two questions are related because active circuits impose a gain-bandwidth limitation, and a further complication arises from the fact that the bandwidth of each stage of a multistage amplifier must be greater than the total amplifier bandwidth.

How does one decide what amplifier bandwidth is sufficient? Suppose that the input waveform is square wave; is frequency response to the ninth or eleventh harmonic sufficient? Amplitude

considerations suggest an affirmative answer, but then one remembers that at the breakpoint frequency not only is the amplitude of the fundamental down 3 dB but also the phase is shifted 45° . Furthermore, the other frequencies contained in the square wave are phase shifted an appreciable amount, also. The conclusion is that a major contribution to distortion in the output signal is from the varying amount of phase shift of the various frequency components contained in the square wave. It seems advisable to consider the problem from a different aspect.

The upper frequency can be determined in terms of the desired output signal rise time. Similarly, the low-frequency breakpoint can be defined in terms of the percentage allowable tilt or slope in the output waveform. This approach is not too unrealistic since both the high- and low-frequency breakpoints of an amplifier are likely to be controlled by RC products, an integrating effect in the former case and a differentiating effect in the second case. Consider the waveform of Fig. 9-6.

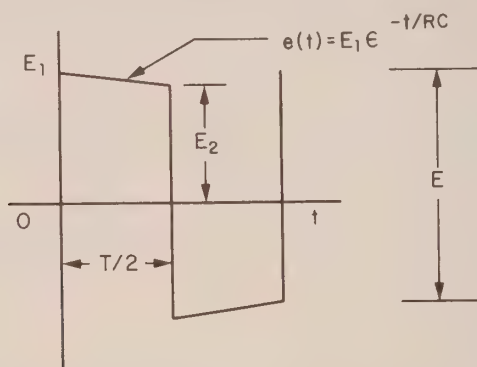


FIG. 9-6 Square Wave - Low-Frequency Distortion

Tilt in the waveform is defined as $(E_1 - E_2)/E$, and one can compute as follows:

Slope of curve for interval $T/2 > t > 0$:

$$\frac{de}{dt} = -\frac{E_1}{RC} e^{-t/RC}$$

Initial slope at $t = 0$:

$$\frac{de}{dt} = -\frac{E_1}{RC}$$

If $RC \gg T$, then the curve is essentially linear, and the voltage

E_2 is found as follows:

$$\begin{aligned} E_2 &= E_1 - \left(\frac{E_1}{RC} \right) \left(\frac{T}{2} \right) \\ &= E_1 (1 - T/2RC) \end{aligned}$$

Eliminating E_2 by utilizing the definition of tilt:

$$\begin{aligned} \text{Tilt} &= \frac{E_1 - E_1 (1 - T/2RC)}{E_1} \\ &= \frac{T}{2RC} \\ \% \text{ Tilt} &= \frac{50T}{RC} \end{aligned}$$

The square-wave repetition frequency f is equal to $1/T$, and the low-frequency breakpoint f_1 is equal to $1/(2\pi RC)$. After making these substitutions, Eq. (9-5) is obtained

$$\% \text{ Tilt} = \frac{100\pi f_1}{f} \quad (9-5)$$

Thus, the low-frequency breakpoint is caused by RC-coupling networks between stages, or, if the stages are direct coupled, the breakpoint may be determined by emitter-bypass circuits. Of course, if the amplifier gain is flat to dc, no low-frequency problem exists.

One can derive quite readily a useful equation for the high-frequency breakpoint if the upper frequency limit is imposed by RC products, i.e., by capacitive loading. The implication is that high-frequency (high gain-bandwidth) transistors are used to implement the amplifier.

A familiar equation describes the output signal of an RC-integrating circuit where the input signal is a step function.

$$e(t) = E(1 - e^{-t/RC}) \quad \text{volts}$$

where $e(t)$ is the output voltage at any time (t), E is the step amplitude, and RC is the integrating time constant.

One can solve for the time interval corresponding to $0.9E > e(t) > 0.1E$, and the result conforms to the definition of rise time. Hence, the following is written:

$$t_r = 2.2RC$$

However, $f_2 = 1/(2\pi RC)$

Therefore:

$$t_r = \frac{2.2}{(2\pi f_2)}$$

$$t_r = \frac{0.35}{f_2} \quad \text{seconds} \quad (9-6)$$

where t_r is the rise time of the output signal in seconds, and f_2 is the high-frequency breakpoint in cps.

Equations (9-5) and (9-6) help in establishing the bandwidth required for a particular video-amplifier application, but another aspect must often be considered as well. That is the effect of bandwidth narrowing. The bandwidth of an amplifier which is composed of several identical stages is less than the bandwidth of an individual stage. Equation (9-7) is useful in accounting for this effect.

$$t_r = \sqrt{t_{rs}^2 + t_{r1}^2 + \cdots + t_{rn}^2} \quad \text{seconds} \quad (9-7)$$

where t_r is the rise time of the output signal, t_{rs} is the rise time of the amplifier input signal, and t_{rn} is the rise time of the n^{th} stage.

9-4 BODE OR LOG MAGNITUDE

Bode or Log-Magnitude techniques are valuable in studying the characteristics of closed-loop control systems. The same techniques are also applicable, in some cases, to circuit analysis and circuit design problems such as simple RC circuits or more complicated circuits like power-supply regulators. One may recall that the criteria for oscillation are a loop gain of at least 1 and a total phase shift of 360° . High-gain power-supply regulators, for instance, often tend to oscillate, and Bode methods are useful in solving such problems.

A simple integrating-type RC circuit, sometimes called a low-pass circuit, is depicted in Fig. 9-7. If the input signal is a step function, the output signal is defined by a well-known equation, $e = E(1 - e^{-t/RC})$. However, if the input signal is sinusoidal,

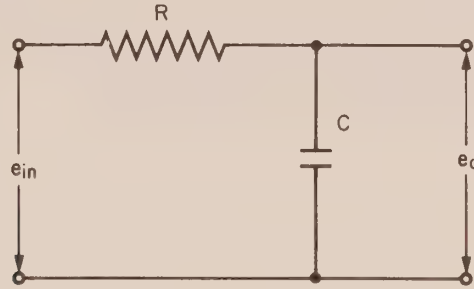


FIG. 9-7 RC Low-Pass Circuit

then the amplitude and phase of the output signal are dependent on the frequency of the input signal. The method of Chap. 3 would yield the following result:

$$\begin{aligned} \frac{e_o}{e_{in}} &= \frac{-jX_C}{R - jX_C} \\ &= \frac{1}{1 + j\omega RC} \end{aligned}$$

Let $T = RC$, then the following transfer function can be written:

$$\frac{e_o}{e_{in}} = \frac{1}{1 + j\omega T}$$

where

$$T = RC$$

$$\omega = \text{Input signal frequency}$$

This equation is complex and indicates amplitude and phase shift of the output signal as a function of ω and T . It is convenient to find the magnitude of the circuit response in dB as a function of ωT . Let K equal e_o/e_{in} . Then, the derivation continues:

$$K = \frac{1}{1 + j\omega T}$$

$$|K| = \frac{1}{\sqrt{1 + \omega^2 T^2}}$$

Taking the logarithm of both sides

$$\log |K| = -\frac{\log(1 + \omega^2 T^2)}{2}$$

But the response in dB is

$$\text{dB} = 20 \log |K|$$

So, multiplication by 20 is necessary.

$$20 \log |K| = -10 \log(1 + \omega^2 T^2)$$

$$\text{dB} = -10 \log(1 + \omega^2 T^2)$$

This equation can be plotted on semi-log paper where the response in dB is plotted on the linear scale, and ω is plotted on the log scale. See Fig. 9-8. The approximate curve is composed of two asymptotes which are straight-line approximations to the actual curve. Note that the actual curve is down 3 dB from the approximate curve at the breakpoint or corner frequency. Above the corner frequency, the response is falling at a rate of 6 dB/octave (20 dB/decade). Also, the output signal is phase shifted from 0 to -90° as the frequency is varied from 0 to ∞ . At the breakpoint frequency, the phase shift is -45° . It is obvious from the curves of Fig. 9-8 that high frequencies are attenuated by any circuit of the type indicated in Fig. 9-7. Hence, such is called a *low-pass circuit*.

A circuit which passes high frequencies and attenuates low frequencies is the same as that in Fig. 9-7 with R and C interchanged. In this case, the equation is:

$$K = 1 + j\omega T$$

The plot is similar to that of Fig. 9-8, but the high-frequency asymptote coincides with the 0 dB line, and the low-frequency asymptote has a positive slope of 6 dB/octave. The two asymptotes intersect as before at the corner frequency ($\omega = 1/T$). Phase shift is $+45^\circ$ at the corner frequency and varies from $+90^\circ$ to 0° as frequency varies from 0 to ∞ . To illustrate, suppose the corner frequency is 600 cps. Then, according to the approximate curve, the response would be down 6 dB from the 600-cps response at a frequency of 300 cps and down 12 dB at a frequency of 150 cps.

Again according to the approximate curve, the response at 1,200 cps would be the same as the response at 600 cps. In the exact case, one could vary the frequency to ∞ or, say to 100×600 cps, and the response would only increase 3 dB from the response at the corner frequency. Another way of describing it is to say that the output amplitude is equal to 70.7% of the input amplitude at the corner frequency, and as frequency is increased toward ∞ , the output amplitude approaches the input amplitude. That is, the capacitor is a short circuit to high frequencies (and an open circuit to dc).

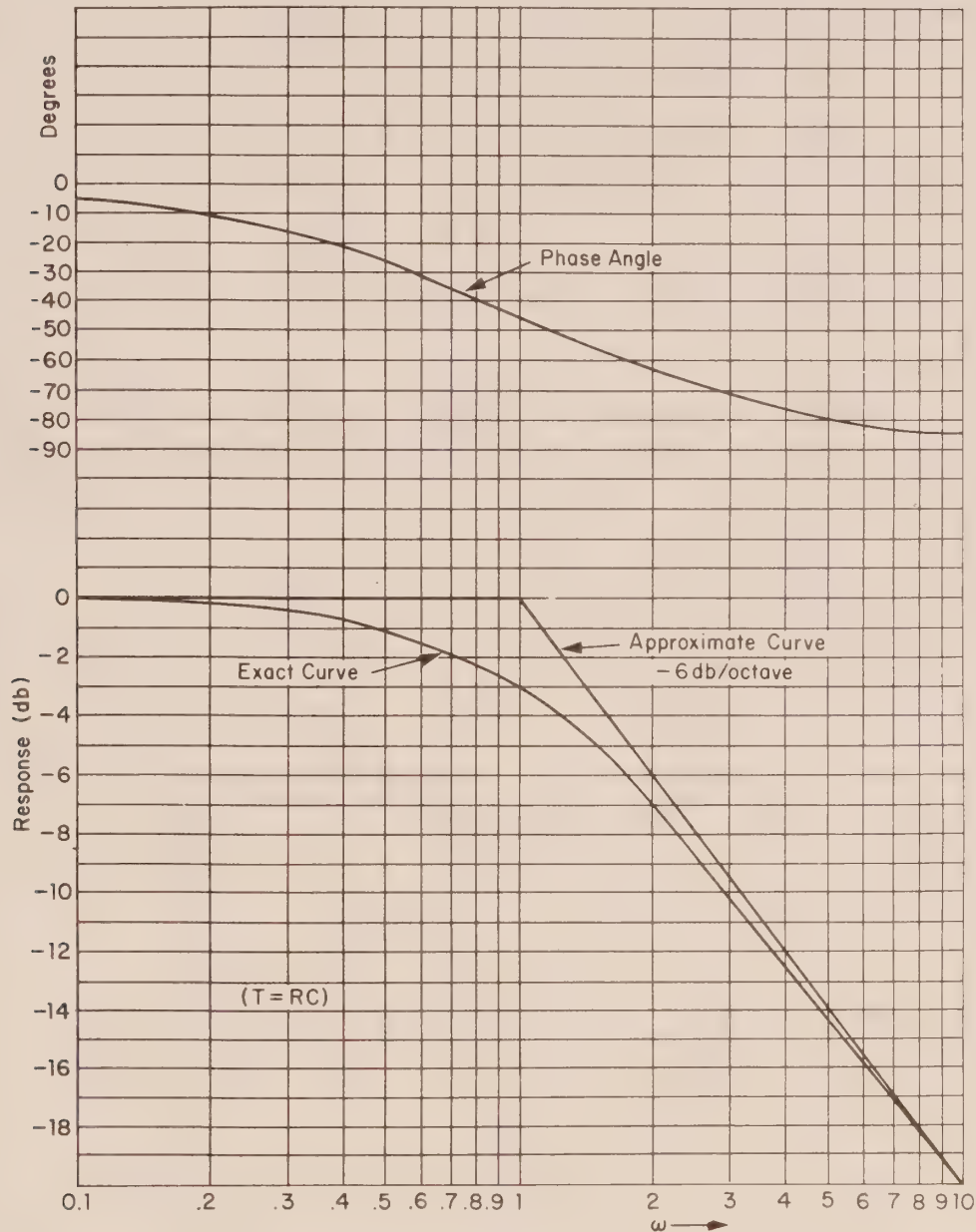


FIG. 9-8 Attenuation-Phase Plot of $\frac{1}{1 + j\omega T}$

9-5 DESIGN EXAMPLE

For best frequency stability, a crystal oscillator must be operated in a temperature-controlled environment, and a small oven is, therefore, to be designed to enclose such an oscillator. In particular, the oven-control circuitry is to be designed, and the following pertinent parameters are listed:

Control Temperature, T_c	100°C Nominal
Required T_c Stability	$\pm 0.1^\circ\text{C}$
Ambient Temperature Range	-25°C to 75°C
Supply Voltage	+20 vdc
Heater-Winding Resistance	50 Ω
Oven-Insulation Coefficient	$75^\circ\text{C}/\text{W}$
Thermistor Resistance @ 100°C	3 k Ω
Thermistor Coefficient @ 100°C	$-2.7\%/^\circ\text{C}$

In this particular case, the control circuitry is to be mounted external to the oven except, of course, for the heater winding and the thermistor which is used in a bridge circuit to detect the oven temperature. The proposed system is as indicated in Fig. 9-9.

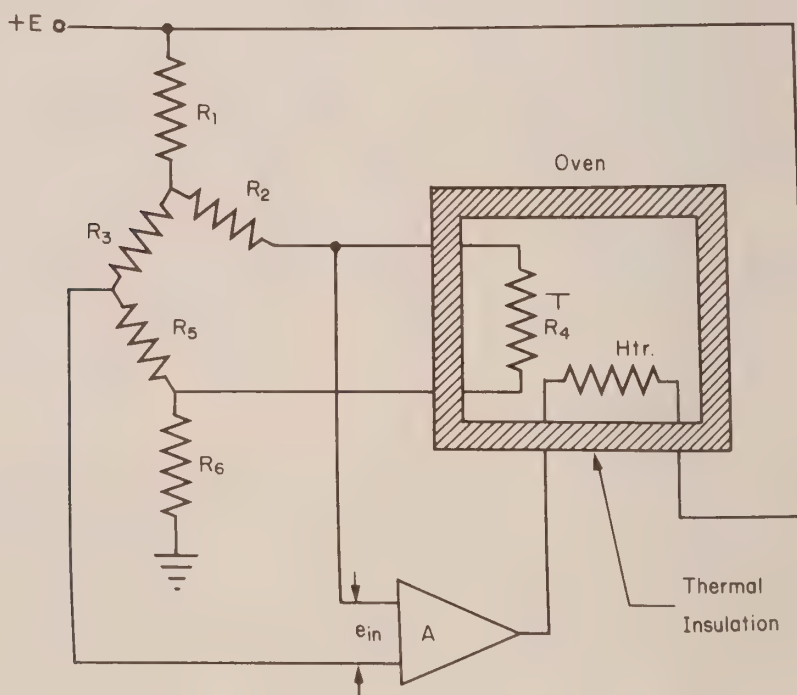


FIG. 9-9 Oven-Control Circuit

From the listed conditions, it is apparent that the control temperature must not change more than 0.1°C for an ambient change of 50°C (variation from 25°C), and the required thermal-loop gain is, then, 500. Several factors affect thermal-loop gain. These are: bridge gain volts/ $^{\circ}\text{C}$, amplifier gain volts/volt, heater-winding factor watts/volt, and oven-insulation coefficient $^{\circ}\text{C}/\text{watt}$. One can write an equation containing the appropriate units:

$$^{\circ}\text{C}/^{\circ}\text{C} = (\text{V}/^{\circ}\text{C})(\text{V}/\text{V})(\text{W}/\text{V})(^{\circ}\text{C}/\text{W})$$

Bridge gain can easily be determined if it is known how e_{in} of Fig. 9-9 varies as a function of R_4 . Equation (9-8) can be written after a number of arithmetical operations are performed:

$$\frac{\Delta e_{in}}{\Delta R_4} \approx \frac{E R_3}{(R_3 + R_5)(R_1 + R_2 + R_4 + R_6) + (R_1 + R_6)(R_2 + R_4)} \quad (9-8)$$

where Δe_{in} and E are in volts and ΔR_4 and all resistor values are in ohms.

It is assumed in the derivation of Eq. (9-8) that the amplifier input impedance is high and that the bridge is always essentially balanced.

It is clear from Eq. (9-8) that the higher the bridge voltage, or alternately the voltage across the thermistor (R_4), the greater is the bridge gain in $\text{V}/^{\circ}\text{C}$. However, for best stability, the power dissipated in the thermistor must be quite low, say less than one mW. Reasonable, but somewhat arbitrary, values are chosen for the bridge resistors as follows:

$$R_1 = 12.1K$$

$$R_2 = 10.0K$$

$$R_3 = 10.0K$$

$$R_4 = 3K \text{ Thermistor}$$

$$R_5 = 3.01K$$

$$R_6 = 5.49K$$

All the bridge resistors are one percent, temperature-stable types. The actual design might require one resistor, say R_5 , to

be variable in order that the oven temperature could be set. Bridge gain is calculated from Eq. (9-8) as follows:

$$\begin{aligned}\frac{\Delta e_{in}}{\Delta R_4} &= \frac{(20)(10)(10^{-3})}{(10 + 3.01)(12.1 + 10 + 3 + 5.49) + (12.1 + 5.49)(10 + 3)} \\ &= 0.32 \times 10^{-3} \text{ volts/ohm}\end{aligned}$$

The thermistor coefficient is $-2.7\%/^{\circ}\text{C}$ or $-81 \Omega/^{\circ}\text{C}$. Therefore, the bridge gain is:

$$\begin{aligned}\text{Bridge Gain} &= (81)(0.32)(10^{-3}) \\ &= 25.8 (\text{mV}/^{\circ}\text{C})\end{aligned}$$

Bridge gain has been calculated, the oven insulation coefficient was given, and the heater winding factor is essentially defined as well, since the supply voltage, heater resistance, and oven insulation coefficient are specified. The only real unknown is the amplifier voltage gain, and it is this factor which is varied to achieve the desired thermal-loop gain of 500.

The heater-winding factor is considered next. Since the control temperature is 100°C which is 75°C above ambient, and the oven insulation coefficient is $75^{\circ}\text{C}/\text{W}$, then one watt must be dissipated in the heater at room temperature. The voltage across the heater resistance is:

$$\begin{aligned}E_R^2 &= PR \\ &= (1)(50) \\ E_R &= 7.07 \text{ volts}\end{aligned}$$

What is desired is the change in heater power as a function of change in voltage across the heater winding:

$$\begin{aligned}P &= \frac{E_R^2}{R} \\ \frac{dP}{dE_R} &= \frac{2E_R}{R} \\ &= \frac{14.14}{50} \\ &= 0.283 \text{ watts/volt}\end{aligned}$$

A complete equation is now written:

$$\text{Thermal-loop gain} = 500 \text{ }^{\circ}\text{C}/^{\circ}\text{C}$$

$$\begin{aligned} 500 \text{ }^{\circ}\text{C}/^{\circ}\text{C} &= (25.8 \text{ mV}/^{\circ}\text{C}) \left(A \frac{\text{V}}{\text{V}} \right) (0.283 \text{ W/V}) (75^{\circ}\text{C/W}) \\ &= 0.55 \text{ A} \end{aligned}$$

The amplifier voltage gain is, then:

$$\begin{aligned} A &= \frac{500}{0.55} \\ &= 910 \end{aligned}$$

One would probably specify an amplifier with an open-loop gain of 10,000 or more and operate it with a closed-loop gain of 1,000.

PROBLEMS

- 9-1 In the differential amplifier circuit of Fig. 9-1, the two transistors have identical characteristics, and the circuit parameters are specified as follows:

$$h_{fe} = 100$$

$$h_{ie} = 5 \text{ k}\Omega$$

$$h_{oe} \cong 0$$

$$R_L = 7.5 \text{ k}\Omega$$

$$R_1 = 2 \text{ k}\Omega$$

$$R_2 = 2 \text{ k}\Omega$$

$$e_1 = 0.01 \sin 2513t \text{ volts}$$

$$e_2 = 0.02 \sin 2513t \text{ volts}$$

- a. What is the amplitude of the ac voltage which appears from collector to collector? Assume linear operation.
- b. Solve part *a* with e_2 redefined as follows:

$$e_2 = 0.01 \sin 2513t \text{ volts}$$

- c. Repeat part *a* with e_2 defined as follows:

$$e_2 = 0.01 \sin(2513t + \pi) \text{ volts}$$

- 9-2 In the operational amplifier circuit of Fig. 9-4, the input impedance (Z_{in}) is composed of a 100 K resistor in series with a 0.01- μ F capacitor and the feedback impedance (Z_f) is a 1.5 M Ω resistor. The amplifier gain (A) can be considered infinite. What is the transfer function (e_o/e_{in})? Are high-frequency signals amplified more than low-frequency signals?
- 9-3 An ideal square wave with a repetition rate of 1,000 pps is the input signal to a video amplifier. What amplifier bandwidth is required if the allowable tilt in the output signal is 5% and the maximum allowable rise time is 1 μ s?

- 9-4 In the circuit of Fig. 9-7, the values of R and C are 130 K and 1 μ F, respectively. What is the response at 120 cps relative to the response at dc?
- 9-5 Design an operational amplifier, of the type depicted in Fig. 9-4, which has an amplitude response e_o/e_{in} identical to that of the circuit of Prob. 9-4. That is, specify Z_{in} , Z_f , and A .
- 9-6 Design a circuit which has the following output-vs.-input characteristic:

$$e_o = -(5 e_1 + 10 e_2) \quad \text{volts}$$

- 9-7 a. Suppose that the input signal to the circuit of Prob. 9-4 were a unit positive-going step (1 V) which occurred at $t = 0$. What would be the equation of the output signal as a function of time, and what would be the amplitude at $t = 0.13$ sec?
- b. Repeat Part a for the amplifier of Fig. 9-4 where Z_{in} is a 130-K resistor, Z_f is a 1- μ F capacitor, and A is infinite. Also, what is the output amplitude after 0.26 sec.?
- 9-8 A video amplifier is required for use with a two-pulse decoder. The input signal, which is depicted in Fig. 1, is 4 mV in amplitude (peak to peak) and exhibits rise and fall times which are essentially 0. Decoder requirements indicate that the rise and fall times of the output signal must be equal to or less than 0.14 μ s. Also, maximum allowable droop between pulse groups is 3 percent. Amplifier output amplitude is to be 2.5 V p-p. The video amplifier is composed of four identical stages.

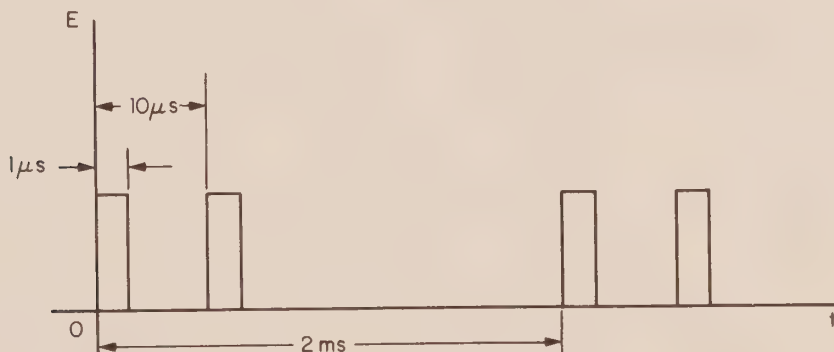


FIG. 1 Two-Pulse Signal

- a. What gain-bandwidth is required from each stage?
- b. Transistors with gain-bandwidth products (f_t) of what should be used in the amplifier if bandwidth is limited by RC products?

9-9 An amplifier with a closed-loop gain of -5 is required. The closed-loop gain must not vary more than ± 1 percent if the open-loop gain is varied ± 50 percent.

- a. What is the minimum magnitude of open-loop gain (A)?
- b. What is the corresponding value of the feedback factor (β)?

BIBLIOGRAPHY

- D'Azzo and Houpis: "Control System Analysis and Synthesis, pp. 178-184, McGraw-Hill Book Company, New York, 1960.
- Landee, Davis, and Albrecht: "Electronic Designers' Handbook," pp. 3-31 to 3-33, 19-45 to 19-48, McGraw-Hill Book Company, New York, 1957.

SWITCHING CIRCUITS

10-1 CLIPPING, LIMITING, AND DC RESTORATION

The subject of this section pertains most generally to non-sinusoidal applications or, more particularly, to pulse and digital circuitry. The concepts associated with clipping, limiting, and dc restoration, although important, are rudimentary in nature. For instance, capacitors and transformers are inherently ac devices which can be used to couple ac signals from one dc level to another. No dc current, in the steady state, conducts through a capacitor and, likewise, for the secondary of a transformer provided that the load impedance is linear and bilateral. That is, ac voltages, with no dc component, are developed across linear, bilateral load impedances when driven from either transformer or capacitor-coupled signal generators.

Certain erroneous conclusions from the foregoing information are possible. One such conclusion might be that, since only ac currents in the steady state flow through a capacitor, only ac voltages can be developed across the corresponding load impedance. This conclusion is not true if the load impedance is unilateral. Consider the circuit of Fig. 10-1.

The output signal is as depicted in Fig. 10-1b if $R_L C \gg t_2$. Quite clearly, there is an average value in the output signal since the indicated negative voltage is equal in magnitude to the voltage drop of a conducting diode, i.e., less than 1 V. Average current through the capacitor is, however, zero and Eq. (10-1) defines the relationship which is required to maintain this condition.

$$i_1 t_1 = i_2 (t_2 - t_1) \quad (10-1)$$

During the time interval from 0 to t_1 , the diode is reverse-biased, but from t_1 to t_2 it is forward-biased and conducting the current i_2 (if R_L is much greater than the diode forward resistance).

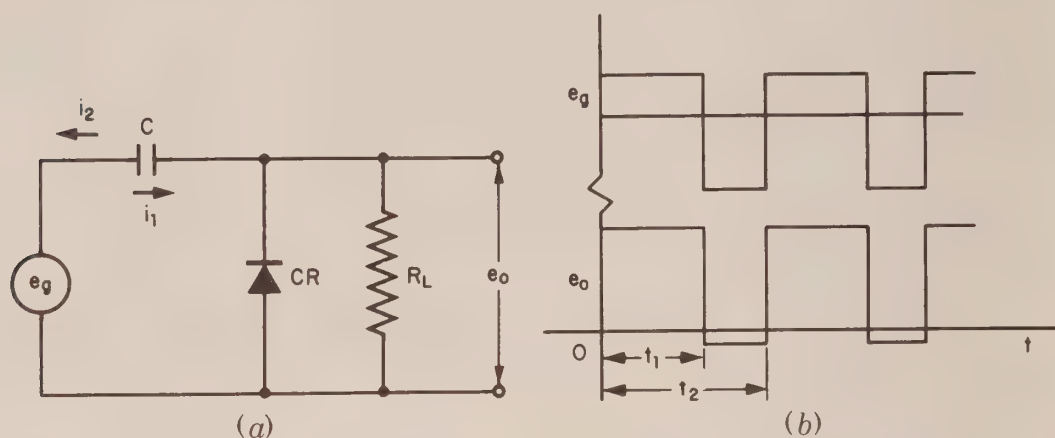


FIG. 10-1 Peak Detector

The circuit of Fig. 10-1 is often used to reference signals to any voltage level including, but not limited to, ground potential. The output signal, for the particular case shown in Fig. 10-1, contains a component of positive dc voltage. Suppose that the anode and cathode of the diode are reversed. What then would be the character of the output signal? It would contain a component of negative dc voltage not equal in magnitude (unless the input signal is symmetrical) to the aforementioned positive voltage. In either case, the signal could be filtered to extract the dc component, and the point is made that positive- or negative-bias voltages can be obtained without the use of transformers.

It is desirable at times, for various reasons, to limit signal amplitudes. A common circuit which is used for such purposes is depicted in Fig. 10-2. Output signal amplitude is limited essentially to the range of $+E_2$ to $-E_1$ volts. Thus, the maximum peak-to-peak output voltage is, for ideal rectifiers, equal to the magnitude of E_2 plus the magnitude of E_1 . The voltages E_1 and E_2 may both be zero in which case the output signal is limited in amplitude to the sum of the two rectifier voltage drops.

Note that peak rectifier currents are high if R_g is small in value. Hence, the indicated circuit works better to limit plate or collector signals than cathode or emitter signals because of the difference in output impedance.

The capacitor in Fig. 10-2 must be large enough in value so that the voltage change across it, during the time interval that either rectifier is forward-biased, is small compared to signal amplitude.

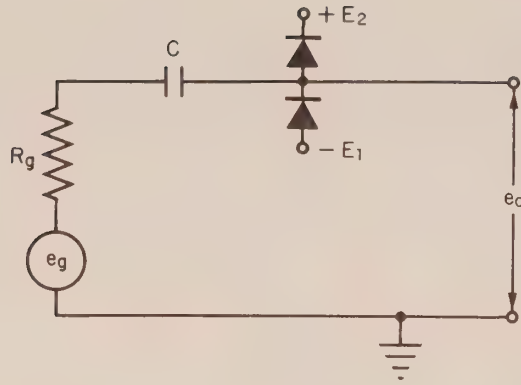


FIG. 10-2 Limiter

10-2 TRANSISTOR SWITCHING CHARACTERISTICS

Characteristics of an ideal switch include zero closed impedance with infinite current-carrying capacity, and infinite open impedance with infinite breakdown voltage. Transistor switching characteristics differ from those of an ideal switch to a considerable degree. Current carrying capacity is limited in the steady state to $(I_c)_{\max}$, for instance, and the voltage rating is limited to V_{CB} (or V_{CEO}). Furthermore, the closed impedance is finite and equal to r_{sat} , and the open-circuit current is at least equal to the collector leakage current I_{co} . However, for most applications, these limitations are not too severe.

Significant circuit problems often arise because of limitations associated with switching speed. Consider an ideal square wave as a control signal for a transistor switch. When the square wave changes from the switch-open to the switch-closed state, the transistor remains in the cutoff (switch-open) state for some length of time (delay time, t_d) before it starts to change state. Then, some length of time (rise time, t_r) is required for the transistor to turn on and transfer from the cutoff to the saturated state. A similar problem exists when the square wave reverses back to the switch-open state; the transistor remains in the saturated state for some length of time which is referred to as *storage time* (t_s). Fall time or turn-off time (t_f) is then required for the transistor to reverse from the saturated to the cutoff state.

Delay time (t_d) is short enough to be neglected for most applications. Rise time (t_r) and fall time (t_f) are proportional to the inverse of ω_a , and, therefore, high-frequency transistors are used for fast switching applications. Perhaps the most frequent switching problem is with storage time (t_s) which occurs when transistors are overdriven or heavily saturated. A solution is to design so that saturation does not occur, but in

production designs overdrive is desirable to ensure that all units work properly. Thus, transistors are sometimes overdriven but clamped out of saturation. One method is depicted in Fig. 10-3.

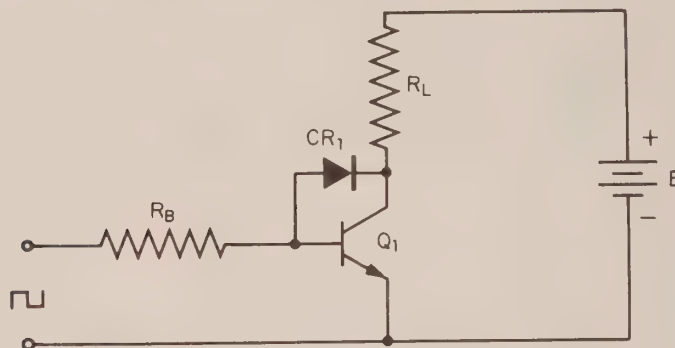


FIG. 10-3 Saturation-Inhibit Circuit

If the forward voltage drop of CR_1 is less than the like drop of the base-emitter diode, then excess base-drive current is conducted through CR_1 and becomes collector current. [Note that $(V_{CE})_{sat} < V_{BE}$.] A frequent combination is for CR_1 to be a germanium diode and Q_1 a silicon transistor.

Storage time increases as forward-base current is increased beyond the value required for transistor saturation. In the saturated state, both the emitter-base diode and the normally reverse-biased collector-base diode are forward-biased, i.e., both diodes are conducting in the forward direction. When the transistor is to be switched to the cutoff state, it is desirable to apply reverse bias, within the associated voltage rating, to the emitter-base diode. In such a case, the emitter-base diode conducts reverse current for some length of time, and storage time is decreased as the magnitude of the reverse current is increased. The point can be stated simply: Transistors are switched more rapidly from the saturated to cutoff state if the turn-off signal reverse-biases the emitter-base diode. A reverse-bias amplitude of 0.2-V or more is sufficient, but one should remember that it is really the amplitude of the reverse current that is important in reducing storage time.

A technique for improving switching response is indicated in Fig. 10-4 where C_2 is the emitter-base capacitance and R_2 is the input resistance.

Equation (10-2) can be derived quite easily if the input and output signals are to be square waves. That is, the output signal is not to be peaked or rounded at the corners. The requirement is that both the dc and ac division ratios be the same:

$$R_1 C_1 = R_2 C_2 \quad (10-2)$$

Equation (10-2) applies not only to transistor circuits but also to any case where broadband matching is necessary. An oscilloscope is an example. Some input impedance in the form of resistance in parallel with capacitance is essentially unavoidable. Matching is achieved by incorporating in the oscilloscope probe a resistor in parallel with an adjustable capacitor. Figure 10-4 and Eq. (10-2) apply to this type of application.

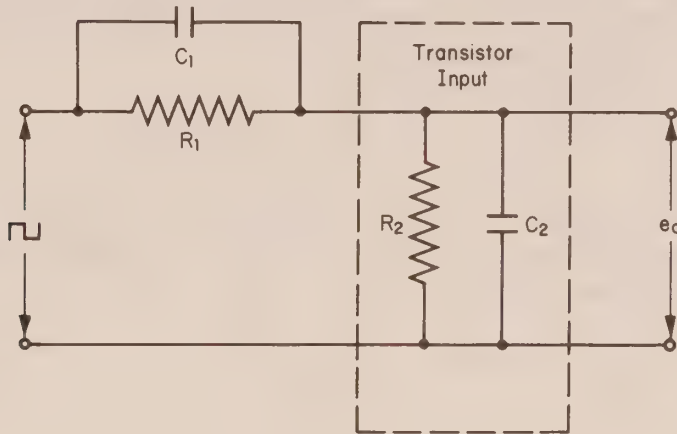


FIG. 10-4 Matching Circuit

In transistor circuitry, capacitor C_1 may be somewhat larger (arbitrarily, say, twice as large) in value as that indicated by Eq. (10-2). Then additional ac turn-on current is available for rapid switching to the on state, and, likewise, ac turn-off current is available when the control signal switches the transistor to the off state.

Appropriate switching characteristics are included in manufacturers' data sheets, and one can use this information as an aid in design.

10-3 MULTIVIBRATORS

Several switching circuits, all of which incorporate positive feedback, are covered in this section. These are: Schmitt trigger, monostable or oneshot multivibrator, astable or free-running multivibrator, and flip-flop. All of the aforementioned circuits are widely used, but, perhaps due to the advent of digital computers, flip-flops dominate in terms of sheer numbers.

Schmitt Trigger

The Schmitt trigger is used to detect dc or slowly varying ac voltage levels. The circuit is characterized by two states,

one for the case where the input signal amplitude is less than the trigger level and one where the trigger level is exceeded. The circuit remains in the off state as long as the trigger level is not exceeded, and, likewise, remains in the triggered state as long as the input signal amplitude exceeds the trigger level. Schmitt triggers exhibit hysteresis. That is, the turn-off signal amplitude is less in magnitude than the turn-on amplitude.

Applications include conversion of sinusoidal signals into square-wave signals and sensing of dc levels. Example 10-1 is used to describe the latter case.

Example 10-1

A Schmitt trigger is to be designed to operate over a temperature range of from -58°F to $+160^{\circ}\text{F}$. Other quantities are specified as follows:

Germanium transistors	(PNP)
Supply voltage	-24 vdc
Load resistance	$2.2\text{ K}\Omega$
$(I_{CO})_{\text{max}}$	$-5\text{ }\mu\text{a}$ @ 25°C
β range	50 to 250 including variations due to temperature.
$(I_C)_{\text{max}}$	-50 mA
Trigger level	Approximately -3.8 V
Source impedance	$2\text{ k}\Omega$

The proposed circuit is depicted in Fig. 10-5, and the task is to solve for the values of R_1 , R_2 , R_3 , and then to verify that the circuit operates properly.

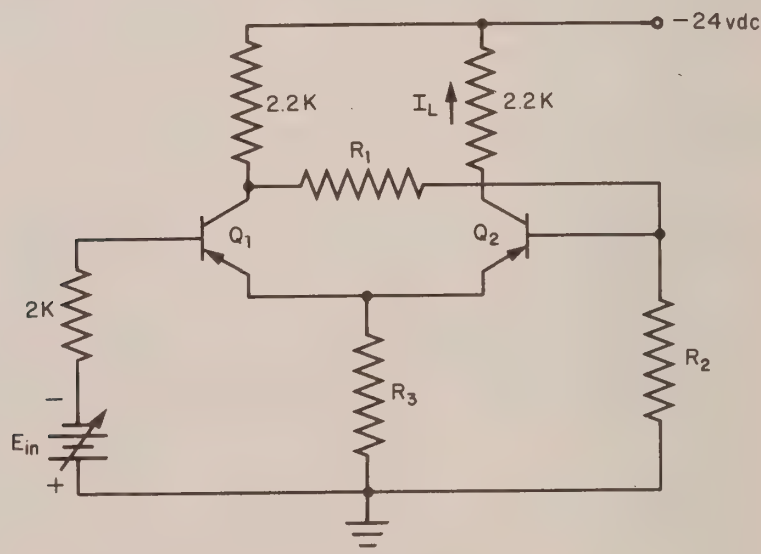


FIG. 10-5 Schmitt Trigger

The design is initiated by setting the voltage drop across resistor R_3 equal to the trigger voltage (-3.8 V) because the circuit will, in fact, trigger when the input level is approximately equal to the emitter voltage of Q_1 . That is, the base-emitter junction of Q_1 must be at least slightly forward-biased before triggering occurs. (To be more exact, one would set the magnitude of the emitter voltage equal to the sum of the magnitudes of V_{EB} , the voltage drop across the 2 K input resistor, and the desired trigger voltage.)

When the input voltage is zero, transistor Q_2 is saturated and transistor Q_1 is cutoff. The saturation voltage $(V_{CE})_{\text{sat}}$ is essentially zero in this case, and, therefore, a value for R_3 can readily be calculated.

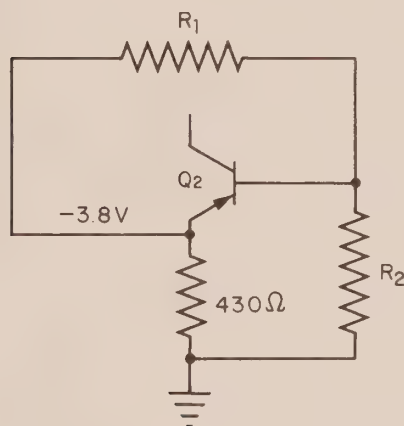
$$3.8 = \left(\frac{R_3}{R_3 + 2200} \right) \quad (24)$$

$$R_3 = 414$$

$$\cong 430\ \Omega$$

Resistors R_1 and R_2 must combine to bias transistor Q_2 into cutoff or saturation depending upon the state of transistor Q_1 .

The following circuit describes the case where Q_2 is to be cutoff.



Cutoff State (Q_2)

It is known from practice that resistor R_1 is considerably larger in value than resistor R_2 . Hence, R_1 is considered infinite for this calculation. It would appear, then, that the emitter-base diode of Q_2 is reverse-biased by 3.8 V. Such is not the case at high temperature, however, because leakage currents (I_{co} and I_{eo}) conduct through R_2 , thereby introducing a voltage drop across this resistor. Since germanium transistors are involved, it is advisable that the

magnitude of reverse bias be at least 1 V. Hence, the leakage-current-induced voltage drop across R_2 must be less than 2.8 V

$$(R_2)_{\text{max}} = \frac{2.8}{I_{co} + I_{eo}}$$

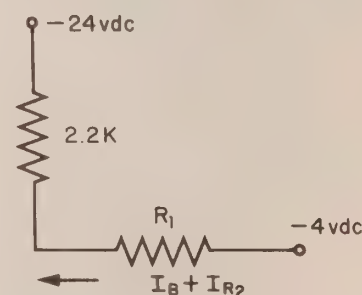
Since data are not given on I_{eo} , it is arbitrarily set equal to I_{co} which is $62 \mu\text{A}$ at 160°F

$$\begin{aligned}(R_2)_{\max} &= \frac{2.8}{2(62)} \text{ M}\Omega \\ &= 22.5 \text{ k}\Omega\end{aligned}$$

Sometimes I_{eo} is ignored since it can be argued that there is no current amplification as long as the emitter-base diode is not forward-biased. When the base-emitter voltage is equal to zero, there is no current conduction from emitter to base and hence no voltage drop in R_2 caused by I_{eo} . However, the current in the collector circuit is somewhat more than I_{CBO} under these conditions.

Another circuit simplification is used as an aid in solving for the value of resistor R_1 . In this case, transistor Q_2 must be biased into saturation, and a voltage level of -4 V at the base is sufficient.

The worst case exists at cold temperatures where I_{co} and I_{eo} are essentially zero.



$$\begin{aligned}I_B &= \frac{I_C}{\beta} \\ &= \frac{24}{(2.63 \text{ K}) \beta} \\ &= \frac{9.1}{50} \\ &= 0.182 \text{ mA}\end{aligned}$$

The voltage drop across resistor R_2 is 4 V , and the maximum value of R_2 is $22.5 \text{ k}\Omega$, which means that the current is approximately 0.18 mA . However, it is always desirable to employ as large a safety factor as possible. Let the value of R_2 be $3.9 \text{ k}\Omega$, which permits the R_2 current to be approximately 1 mA

$$R_2 = 3.9 \text{ k}\Omega$$

A value for resistor R_1 can now be calculated from the available data

$$(R_1)_{\max} = \frac{24 - 4}{1.2 \text{ mA}} - 2.2K$$

$$= 15 \text{ k}\Omega$$

One could specify a value for resistor R_1 less than $15 \text{ k}\Omega$ to improve the safety factor, but worst-case β (50) was used, and the $15K$ value is retained in this case.

Temperature Effects

The temperature-dependent variations of the pull-in voltage are due, for the most part, to variations in V_{BE} of transistor Q_1 . This variation is calculated as follows

$$160^\circ\text{F} = 71^\circ\text{C}$$

$$\Delta T = 71^\circ - 25^\circ$$

$$= 46^\circ\text{C}$$

$$\Delta V_{BE} = -(2 \text{ mV}/^\circ\text{C})(46^\circ\text{C})$$

$$\cong -0.1 \text{ volt}$$

One would predict, then, that the absolute value of the pull-in voltage would *decrease* by about 0.1 volt at 160°F . A similar calculation for the -58°F case indicates that the pull-in voltage increases by 0.15 volt.

Further calculations are possible. Dropout voltage, the effect of leakage currents conducting through R_3 and the 2-K input resistor, etc. could be analyzed. However, a more satisfying experience would be to build and test the circuit, and it was, in fact, constructed with 5%-carbon-composition resistors with the following results:

	Calculated	Experimental
Pull-in (25°C)	-3.8 V	-3.75 V
Pull-in (71°C)	-3.7	-3.65
Dropout (25°C)		-2.7
Dropout (71°C)		-2.3

A comment is worth noting: The output signal from the collector of Q_2 is snap-acting, i.e., bistable, but the equivalent

signal at the collector of Q_1 is not because, for slowly varying input signals, Q_1 operates in the linear region until Q_2 begins to conduct thereby providing positive regeneration.

Oneshot Multivibrator

Two states, one stable and the other transitory, are associated with oneshot multivibrators. A short-duration input pulse triggers the oneshot into the transitory state, and it remains in this state for a period of time which is essentially dependent only on an RC product. Thus, each time it is triggered, the oneshot generates a pulse of given width. The output signal can be differentiated and a pulse obtained which is coincident in time with the trailing edge of the oneshot signal. Both, of course, are delayed from the trigger signal by the period of the oneshot multivibrator. In fact, the oneshot is used to generate a signal which is delayed from some other switching signal. Another application is for generation of gating or reset signals.

The period of a oneshot, i.e., time in the transitory state is set by the design, and considerable latitude is possible. The period may range from approximately one-half microsecond to several seconds. Consider the circuit of Fig. 10-6.

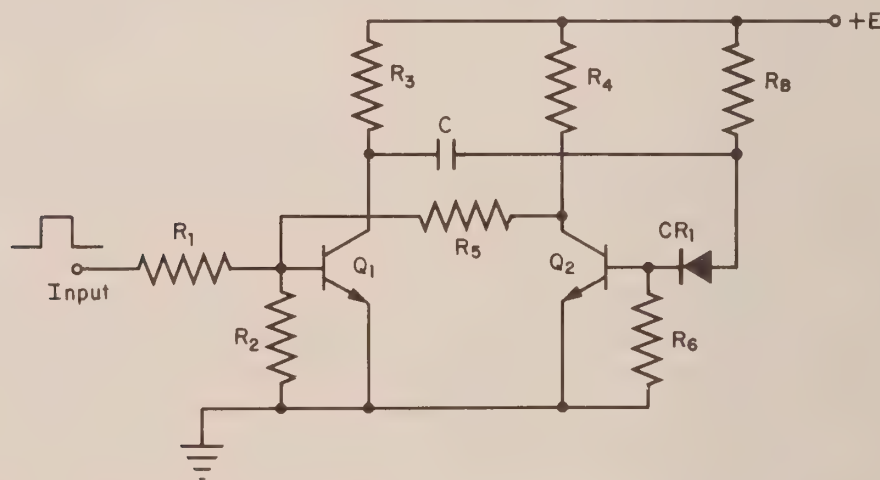


FIG. 10-6 Oneshot Multivibrator

In the stable state, transistor Q_2 is biased into saturation by dc current through resistor R_B , and transistor Q_1 is cutoff since no forward bias is applied. It is assumed for the rest of this discussion that leakage current (I_{co}) and saturation voltage (V_{sat}) are both zero—a valid assumption for modern silicon switching transistors. The circuit can be triggered into the transitory state either by momentarily turning Q_1 on or by turning Q_2 off. Suppose that Q_1 is switched on. Then, a negative going step,

E volts in amplitude, occurs at the collector of Q_1 and is cross-coupled by C to the anode of CR_1 . A key waveform, indicated by Fig. 10-7, occurs at the anode of CR_1 .

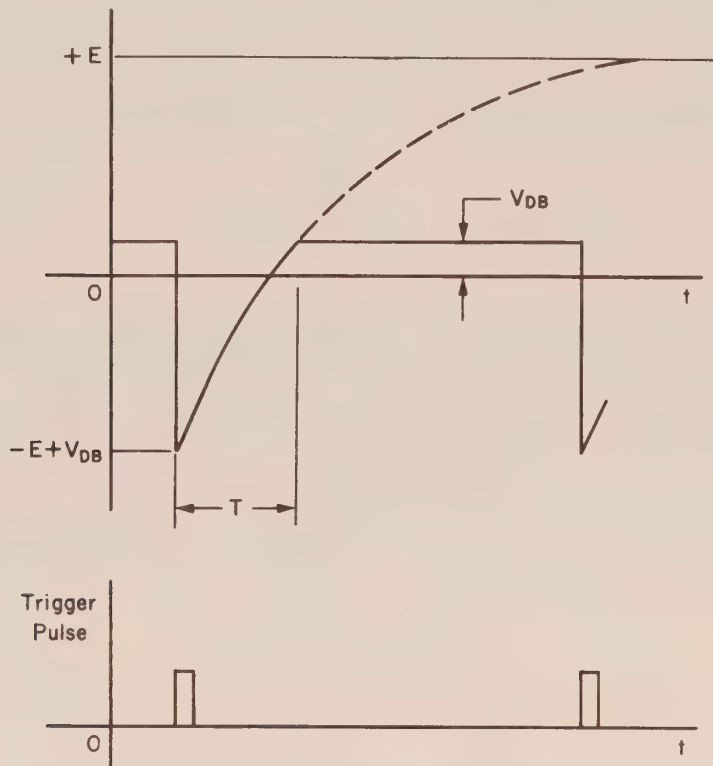


FIG. 10-7 Waveform at Anode of CR_1

The need for diode CR_1 is apparent from the curve of Fig. 10-7. A negative peak signal, which is almost equal to E volts in magnitude, occurs at the anode of CR_1 . If the diode were shorted, then this waveform would appear at the base of Q_1 thereby reverse-biasing the emitter-base junction. Since the reverse emitter-base voltage rating is normally quite low, voltage breakdown would likely occur with the result that the period T would be shortened and the transistor possibly damaged. Although the diode prevents reverse biasing of the emitter-base diode, transistor (Q_2) is switched off by the removal of forward bias.

The symbols in Fig. 10-7 are identified as follows: T is the oneshot period, E is supply voltage magnitude, and V_{DB} is the sum of V_{BE} and the drop across diode CR_1 (forward-biased). One can solve for the period T more easily, perhaps, if the waveform in Fig. 10-7 is referenced differently. Let the minimum voltage be zero, the voltage level where regeneration back to the stable state occurs be E , and the voltage level toward which the capacitor is charging be $2E - V_{DB}$. Then, one can solve for T as follows

$$\frac{E}{2E - V_{DB}} = 1 - e^{-T/RC}$$

$$\frac{1 - V_{DB}/E}{2 - V_{DB}/E} = e^{-T/RC}$$

$$e^{T/R_B C} = \frac{2E - V_{DB}}{E - V_{DB}} \quad (10-3)$$

Tables of e^x and e^{-x} are often available, and Eq. (10-3) is therefore in a useful form. If V_{DB} is 0 or much less than E , Eq. (10-3) can be reduced to approximate Eq. (10-4)

$$T \cong 0.7 R_B C \text{ seconds} \quad (10-4)$$

Eq. (10-3) can be solved for T by taking natural logarithms

$$T = R_B C \left[\ln \left(\frac{2E - V_{DB}}{E - V_{DB}} \right) \right] \text{ seconds} \quad (10-5)$$

The next pertinent question relates to period stability vs. temperature. Is the period of a one-shot stable if ambient temperature is varied? The answer in gross terms is that period stability of ± 1 percent is obtainable without major temperature-compensating circuits over a temperature range of from -40°C to 100°C . Temperature-stable resistor and capacitor types are, of course, required to achieve such results. Suppose that the RC temperature coefficient is zero. What, then, would be the period variation vs. temperature? The factor in Eq. (10-5) that is temperature-dependent is V_{DB} . Therefore, a partial derivative is taken with respect to V_{DB} to find the temperature-dependence of T

$$\frac{\partial T}{\partial V_{DB}} = R_B C \left(\frac{-1}{2E - V_{DB}} + \frac{1}{E - V_{DB}} \right)$$

$$\cong \frac{R_B C}{2E}$$

$$\Delta T = \frac{(R_B C)(\Delta V_{DB})}{2E}$$

A desirable and useful form is one where percentage change in period is expressed as a function of temperature change in degrees centigrade. A solution for initial T is necessary and this can be obtained from Eq. (10-4) or, if greater accuracy is desired, from Eq. (10-5) after some simplifying assumptions. Assume that silicon components are involved and that V_{DB} is, therefore, approximately 1 V. Let the supply voltage be a typical value such as 15 V. The solution for T is, then

$$T = 0.73 R_B C \text{ seconds} \quad (10-6)$$

Equation (10-6) is perhaps the most useful equation for finding period in a circuit such as that depicted in Fig. 10-6. The accuracy involved is approximately 3 percent if silicon components are used, the supply voltage is within a range of from 10 V to 20 V, and the RC product is known accurately.

The derivation of an equation which describes period sensitivity to temperature continues

$$\Delta T = \frac{(R_B C)(\Delta V_{DB})}{2E}$$

$$\frac{\Delta T}{T} = \frac{(R_B C)(\Delta V_{DB})}{(0.73 R_B C)(2E)}$$

$$= \frac{0.685(\Delta V_{DB})}{E}$$

Temperature sensitivity of V_{DB} is approximately $-4 \text{ mV}/^\circ\text{C}$. Equation (10-7) describes the variation of the period of a one-shot multivibrator vs. temperature due to changes in V_{DB} . Actual period variation is somewhat greater than that indicated by Eq. (10-7) because of leakage currents and saturation voltage effects. See the section on astable multivibrators

$$\% \text{ change in } T = \frac{-0.3 \Delta T_C}{E} \quad (10-7)$$

where T is oneshot period, ΔT_C is change in temperature in $^\circ\text{C}$, and E is supply-voltage amplitude.

It must be remembered that a temperature coefficient is associated with the RC product, as well, and the variation from this source must be added to the variation obtained from Eq. (10-7). Note from Eq. (10-3) that T is directly proportional to RC and is independent of E if V_{DB} is 0 and essentially independent otherwise. That is, period remains essentially constant as the supply voltage is varied over wide limits.

Output signals can be taken from either collector, but period varies if the Q_1 signal is attenuated with an external load impedance thereby decreasing the amplitude of the cross-coupled signal. Waveforms are different at the two collectors, also. The Q_1 signal is negative going with essentially a square corner. That is, transistor Q_1 is rapidly switched from the off to the on state, and, in the on or saturated state, it presents a low impedance. However, at the conclusion of the transitory state, Q_1 is switched to the off or high-impedance state, and the collector waveform is then controlled by an RC product (R_3C). Thus, the signal rise time at the collector of Q_1 is relatively slow and is given approximately by Eq. (10-8)

$$t_r = 2.2 R_3 C \text{ seconds} \quad (10-8)$$

The waveform at the collector of Q_2 is a positive-going pulse. The fall time is short because Q_2 rapidly switches to the on condition at the termination of the transitory state. Rise time is relatively fast too since there is little capacity-to-ground loading of the Q_2 signal.

Astable Multivibrator

This multivibrator is used for frequency generation. It is similar to any other oscillator except for the output signal which is essentially of square waveform. Astable multivibrators are often the basis for voltage-controlled oscillators (VCO). In this type oscillator, the output frequency is varied, generally in a linear fashion, by an external dc voltage.

The circuit engineer must not only be capable of designing circuits but also of analyzing them. Hence, the design depicted in Fig. 10-8 is to be analyzed.

The semiconductors are silicon types, and the tolerance associated with either capacitor is ± 1 percent. The transistors are supposed to be biased into saturation, so this condition is checked first. Saturated collector current is obviously 2 mA for a supply voltage of 15 V. The problem, then, is to solve for dc base current. When the base-emitter junction of either transistor is forward-biased, the current through the associated

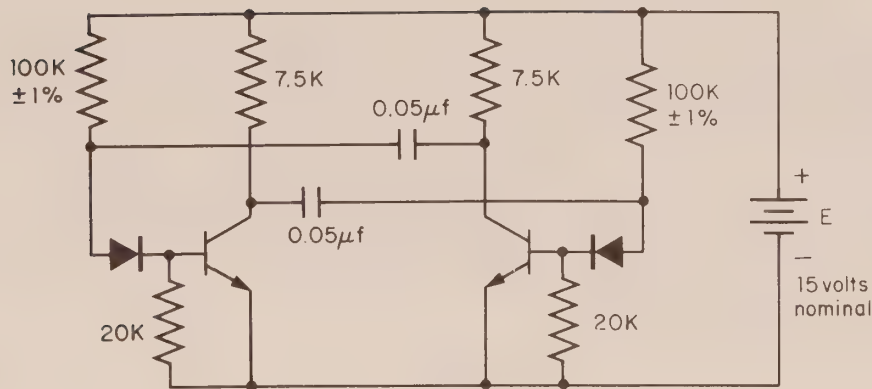


FIG. 10-8 Astable Multivibrator

100-K resistor is

$$I = \frac{15 - 1}{100\text{ K}}$$

$$= 140\text{ }\mu\text{A}$$

The current through the associated 20-K resistor is

$$I_R = \frac{0.5}{20\text{ K}}$$

$$= 25\text{ }\mu\text{A}$$

Hence, the available base current is the difference between I and I_R or $115\text{ }\mu\text{A}$. Minimum allowable β is:

$$\beta_{\min} = \frac{2}{0.115}$$

$$= 17$$

Another factor of interest is collector leakage current I_{co} . This current should not be amplified, otherwise the multivibrator frequency would vary rather drastically with temperature variations. The 20-K resistors are included to prevent amplification of I_{co} . The object is to allow I_{co} to conduct through the associated resistor rather than through the transistor base-emitter junction. Very little current is conducted through the base-emitter junction if the forward bias is less than 0.4 V (for silicon transistors). In the present case, the following I_{co} is tolerable

$$(I_{co})_{\max} = \frac{0.4}{20\text{ K}}$$

$$= 20\text{ }\mu\text{A}$$

Since I_{co} is of the order of $0.1\ \mu\text{A}$ at room temperature, the circuit should operate properly at elevated temperatures.

Period can be found from the oneshot equation (Eq. (10-6) if a modification is made to account for both RC products in the astable circuit. In the present case, symmetry exists, and it is, therefore, only necessary to change the 0.73 number to 1.46. Equation (10.9) describes the frequency of an astable multi-vibrator of the type depicted in Fig. 10-8

$$f = \frac{0.685}{RC} \text{ cps} \tag{10-9}$$

The circuit under consideration should oscillate at the following frequency

$$\begin{aligned} f &= \frac{0.685}{(10^5)(0.05)(10^{-6})} \\ &= 137 \text{ cps} \end{aligned}$$

The unit was constructed with $\pm 1\%$ timing resistors and $\pm 1\%$ capacitors. All other resistors were $\pm 5\%$ carbon composition types. A temperature test was conducted with the RC timing components external to the oven. Table 10-1 indicates the results.

Table 10-1

<i>E</i> volts	<i>T</i> °C	<i>f</i> cps	% Δ <i>f</i>
10	25	137.0	− 2.3
15	25	140.2	—
20	25	141.6	+ 1.0
15	− 25	137.8	− 1.7
15	+ 75	142.8	+ 1.9

For a 50° change in temperature, one would predict from Eq. (10-7) a frequency variation of one percent. The test results indicate a greater variation, and this is attributed to changes in leakage currents and saturation voltage. The nominal-voltage, room-temperature frequency calculations agrees with the experimental result to within 2.3 percent, however.

Outputs can be taken from the collector of either transistor. However, frequency variation occurs if either output signal is attenuated by an external load. Signal rise time is given by

Eq. (10-8) and is 0.825 ms in this case. Fig. 10-9 depicts the waveform at either transistor collector.

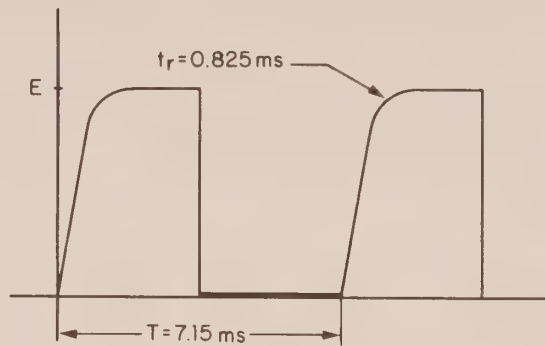


FIG. 10-9 Multivibrator Waveform

To obtain high-frequency operation, it may be necessary to connect capacitors of low value, say equal to 5 percent of either timing capacitor value, across each diode. Transistor storage time is reduced by this technique, and higher frequency operation is, therefore, allowed.

Bistable Multivibrator

As the name suggests, two stable states are associated with the bistable multivibrator. Furthermore, it must be triggered from an external source to induce a change in state. Although all such multivibrators or flip-flops are characterized by two stable states, there are several different kinds which are differentiated by the input triggering requirements. For instance, there are trigger or binary flip-flops, set-reset (RS) flip-flops, and *JK* flip-flops.

One input line is associated with the binary flip-flop, and the device changes state with each input signal. The RS flip-flop, on the other hand, has two input lines, set and reset. A signal on the set line sets the flip-flop to the one state, and, similarly, a signal on the reset line resets it to the zero state. Simultaneous signals on the set and reset lines are not logically allowed. That is, if such happens, the flip-flop state is not defined. *JK* flip-flops are similar to RS flip-flops except that, if simultaneous signals appear on the *J* line and the *K* line, the flip-flop changes state. This flip-flop may be mechanized with a third input line for the purpose of making it act as a binary flip-flop.

Although simple discrete-component flip-flops are usually of the two-transistor type, integrated circuit flip-flops may be composed of several transistors and a number of diodes. One small

integrated circuit may contain several flip-flops, input and/or output buffers, and various logic circuits. Additionally, clear, preset, and clock-pulse input lines make these devices quite versatile. For instance, a divide-by-ten counter is available in the equivalent of a standard transistor can (TO-5 size).

A conventional, discrete-component flip-flop is depicted in Fig. 10-10.

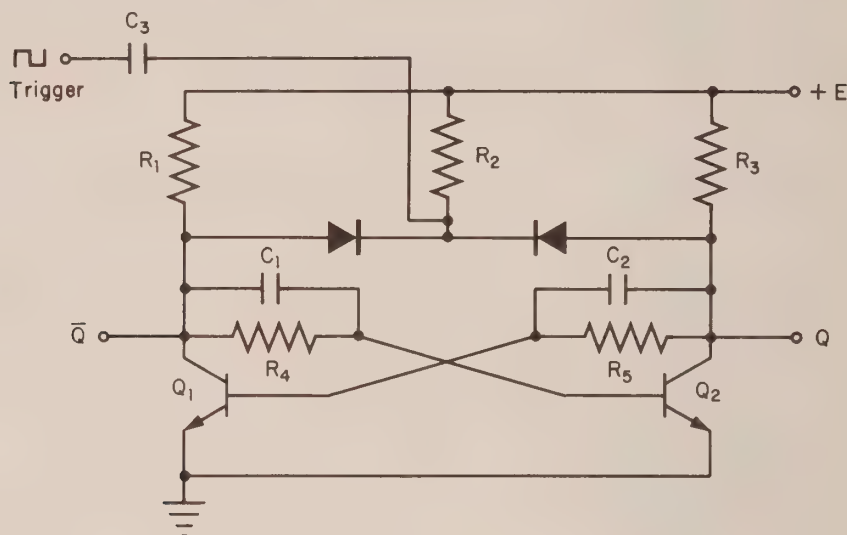


FIG. 10-10 Binary Flip-Flop

If the circuit of Fig. 10-10 is to be designed for a given application, the first parameter that must be known is the input frequency, i.e., what is the count rate? The complete design, including transistor selection and values of resistors and capacitors, depends upon the maximum required count rate. The next and related consideration involves the value of resistors R_1 and R_3 (they are usually equal in value). These resistor values are a function of maximum count rate, available power, external load to be driven, and transistor characteristics particularly relating to current gain vs. emitter current as well as gain bandwidth vs. emitter current.

Suppose that the input signal is a square wave with a repetition rate of 300 cps. Then the task is relatively simple because of the low counting rate. A silicon transistor type with the following characteristics is selected

$$f_T = 100 \text{ mc}$$

$$h_{FE} = 100$$

The first step is to establish the dc requirements, i.e., solve for or select values for R_1 , R_3 , R_4 , and R_5 . System supply

voltage is +20 V dc, and the transistor characteristic curves indicate that an operating current between 2 and 5 mA is advisable. Resistors R_1 and R_3 are, therefore, chosen to be 7.5 k Ω each.

It would seem to be a simple matter to calculate values for resistors R_4 and R_5 , and it is, but several factors are involved. When transistor Q_2 is saturated, transistor Q_1 is supposed to be cutoff. In this state, the Q_1 base resistor (R_5) is connected through a saturated transistor to ground. However, if R_5 is very large in value, the Q_1 collector current is $(h_{FE} + 1)I_{co}$ which may be rather large. If operation at high temperatures is necessary, resistors between each transistor base and ground may be included to allow a path for I_{co} other than through the associated base-emitter diode. These resistors may, in fact, be returned to a negative voltage if such is available.

Thus, resistors R_4 and R_5 should not be excessively high in value, but, on the other hand, they load the output signal and should not be too low in value either. If the resistors were shorted, the output-signal amplitude would be limited to approximately 0.7 V peak to peak. Somewhat arbitrarily, 100 k Ω is selected as the value for both R_4 and R_5 . Note that this value is much less than $(h_{FE})(R_1)$; so saturation of the "on" transistor is assured, and the "off" transistor remains off at relatively high temperatures.

To establish the function of the two diodes and capacitors C_1 and C_2 , it is necessary to examine the sequence of operations. Suppose that transistor Q_2 is on and that transistor Q_1 is off. Then the collector voltage of Q_1 is high, and the like voltage of Q_2 is low. Let a negative-going transition occur on the input line. This transition, because of the assumed flip-flop state, will appear at the collector of Q_1 and be coupled to the base of Q_2 by C_1 . This base signal will switch Q_2 off causing a positive-going signal at the collector of Q_2 . The collector signal will be cross-coupled to the base of Q_1 thereby providing a turn-on signal to that transistor, and positive regeneration will, then, occur with the result that Q_1 becomes saturated and Q_2 cutoff. Thus, it can be seen that the diodes perform a steering operation. That is, negative-going transitions of the input signal are coupled through the appropriate diode to the collector of the off transistor. Capacitors C_1 and C_2 provide a memory function for the flip-flop and allow faster switching by coupling the proper turn-on and turn-off signals to the two transistors.

Consider the case where Q_1 switches from off to on. A large negative-going signal is coupled to the base of Q_2 , and the base-emitter junction of Q_2 should remain reverse-biased until the input signal at the junction of the two diodes decays to

zero. This avoids any possibility of double-triggering. However, the base voltage should also have decayed to zero before the next negative-going transition of the input signal. The minimum value for capacitors C_1 and C_2 can be determined from Sec. 10-2 and Eq. (10-2) if the transistor input characteristics are known. However, the clock frequency is so low (300 cps) that switching speed is not too important. Therefore, capacitors C_1 and C_2 are likely to be much larger in value than the minimum allowable. The question is, basically, how large can they be?

A negative-going transition occurs every 3.33 ms. The discharge path for C_1 is through R_4 , and the like path for C_2 is through R_5 . Also, it is known that, after four RC time constants, a capacitor will be discharged to within approximately two percent of the final value. Thus, one can write the following equation

$$4 R_4 C_1 \leq 3.33 \text{ ms}$$

The solution for the maximum value of C_1 (or C_2) is $0.008 \mu\text{F}$. High-value capacitors tend to be large in physical size, as well, and one would, therefore, choose the lower acceptable value to minimize the space required to package the circuit. A reasonable value for the cross-coupling capacitors (C_1 and C_2) is $0.001 \mu\text{F}$. Thus, the turn-off base signal will last for the following period of time if voltage breakdown of the base-emitter diode does not occur

$$\begin{aligned} 4RC &= (4)(100\text{K})(0.001)(10^{-6}) \\ &= 0.4 \text{ ms} \end{aligned}$$

The time constant of the input differentiator ($R_2 C_3$) should be considerably less than 0.4 ms. One can write the following arbitrary relationship:

$$C_1 R_4 \geq 3R_2 C_3$$

It is only a matter of choosing a combination of R_2 and C_3 , and one choice is $10 \text{ k}\Omega$ and $0.0033 \mu\text{F}$.

One should note that the input differentiator does not operate in a symmetrical manner because the shunt resistance for the negative transitions is the parallel combination of either R_1 and R_2 or R_2 and R_3 , whereas the equivalent load for positive transitions is simply R_2 .

Output signal rise time at either the Q or $\bar{Q}$ output is given by Eq. (10-8) where the RC product is essentially $(7.5\text{K})(0.001 \mu\text{F})$ or $7.5 \mu\text{s}$. Incidentally, the output frequency is one-half the input frequency, i.e., the circuit divides by two.

10-4 LOGIC

Books have been written on the subject of logical design, and it is not the purpose here to condense such material into one section. The object is, rather, to describe certain common operations and gates such as AND, OR, NOR, and NAND.

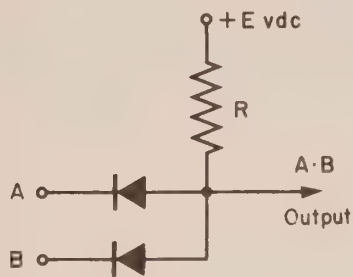


FIG. 10-11 Two-Input AND Gate

Logical gates perform, essentially, a yes-no operation, and when a number of such gates are combined with memory elements like flip-flops, complex problems can be solved. Logical levels are normally defined in two states; a low level is false, and a high level is true. Voltage levels between the two defined levels are not allowed. Consider the circuit of Fig. 10-11.

Inputs A and B must be in one of two states, either 0 volts or $+E$ volts. It is readily apparent that both input signals must be high for an output to occur. Thus, the circuit is an AND gate.

Although the circuit, as depicted, is simple and does operate, a number of practical factors have been ignored. The input levels are generally greater than zero volts and less than E volts, the diode drops are finite, and some capacitive loading of the output is always present. When the input AND condition is realized, it is the pull-up resistor R which causes the output voltage to rise toward $+E$ volts. Thus, this resistor should be small in value to reduce delays and allow high-speed operation, but the smaller it is the greater the current is when the gate is pulled to the 0 state. One solution is to make the voltage E quite high and use a diode to clamp the output to a second voltage less than E in magnitude. Then the output rises toward E and is limited when it reaches the clamping voltage. Gate delay is reduced by this technique.

If a transistor inverting state is connected to the output of the AND gate, the output from the inverter will be a not AND or NAND signal. Such would be written as $\overline{A \cdot B}$.

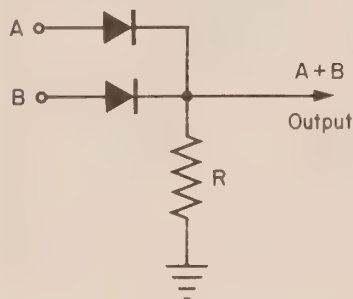


FIG. 10-12 Two-Input OR Gate

If an output is desired when one or more input signals is in the true state, then an OR gate is used. A simple two-input OR gate is depicted in Fig. 10-12.

It is apparent that a true output exists when either A or B is high. In actual practice, resistor R is likely to be returned to a negative supply voltage and the output clamped to ground with a diode.

Again, one can generate the NOT or NOR signal with an inverter. In this case, the inverter output would be designated as $A + B$.

Means other than diodes are available for constructing AND/OR gates. For instance, consider the transistor OR gate in Fig. 10-13.

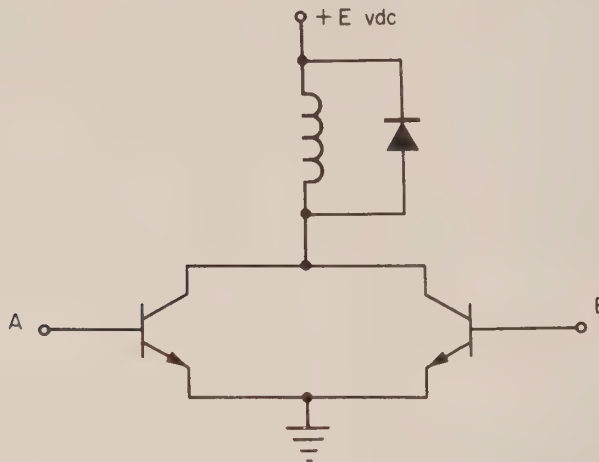


FIG. 10-13 Two-Transistor OR Gate

The relay is activated when either input A or B is in the true state. Since the relay may be a multiple-pole, double-throw type, outputs in the form of contact closures are available for both $A + B$ and $A + B$. Because relay operate and release times are of the order of 5 ms, low-speed operation is dictated for such circuits.

Transistor AND gates can be mechanized by connecting the transistors in series with the load. Combinations of PNP and NPN types are used to satisfy the AND condition, in some cases.

The foregoing information is general and is useful for the occasional circuit problem. Many other factors are involved, however, when complex or high-volume systems are required. For instance, how many levels of logic are allowed, i.e., does one diode gate drive another or does each gate output require a buffer? How many gates can be driven from one buffer? How many input gates per buffer are allowed? Also, what are the propagation delays per gate? Where a great number of logical circuits are involved, each circuit type is likely to be standardized and used repeatedly in the complete system.

10-5 TIME-DELAY CIRCUITS

Electronic systems often require, for various reasons, time-delay intervals of from a few seconds to several minutes.

Programmers or sequencers generate, typically, long AND/OR multifunction delay intervals. This section is concerned with the single-function circuit (that is, a circuit where a single event occurs sometime after the application of power or the reception of an input signal).

The oneshot multivibrator is an example of a delay device where the time delay is a function of an RC product. Perhaps the most simple, and yet practical, time-delay circuits are implemented with unijunction transistors. This transistor consists

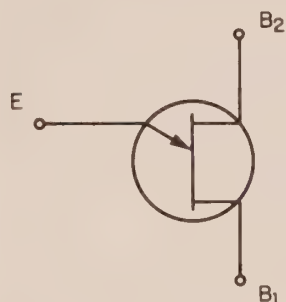


FIG. 10-14 Unijunction Transistor

of a silicon bar mounted between two ohmic base contacts with an emitter junction nearer base 2 than base 1 (see Fig. 10-14). Thus, one junction, where the emitter is of P material and the bar is of N material, is associated with the device.

Operation is described as follows: Base 2 is positive with respect to base 1 causing current to conduct from base 2 to base 1. Since the bar is of ohmic material with an approximate interbase resistance of $10\text{ k}\Omega$, a voltage gradient exists between bases.

Approximately six-tenths of the interbase voltage is present at the point where the emitter is attached to the bar. This fraction, $6/10$, is referred to as the *intrinsic standoff ratio*, η . If the emitter lead is connected to base 1, then the PN junction is reverse-biased, and the device acts like an ordinary resistor. However, if the emitter is connected to a voltage source the output of which is equal to or slightly greater than six-tenths of the interbase voltage, current conducts from the emitter to base 1. The result is that the device enters a negative resistance region of operation where the resistance between the emitter connection and base 1 decreases, which causes increased emitter current and positive regeneration. The emitter current must be reduced below some specified value before the device returns to the original state.

The time-delay possibilities are apparent if a fixed voltage is connected between bases and the emitter driven by a sawtooth waveform. A typical circuit is depicted in Fig. 10-15.

After the switch is closed, the capacitor starts charging toward E volts with a time constant of essentially R_1C since the reverse emitter leakage current is quite low. The voltage at which the unijunction "fires" is given approximately by Eq. (10-10):

$$V_F \cong I(R_3 + \eta R_{BB}) \quad \text{volts} \quad (10-10)$$

where η is the standoff ratio, R_{BB} is the interbase resistance, and I is equal to $E/(R_2 + R_3 + R_{BB})$.

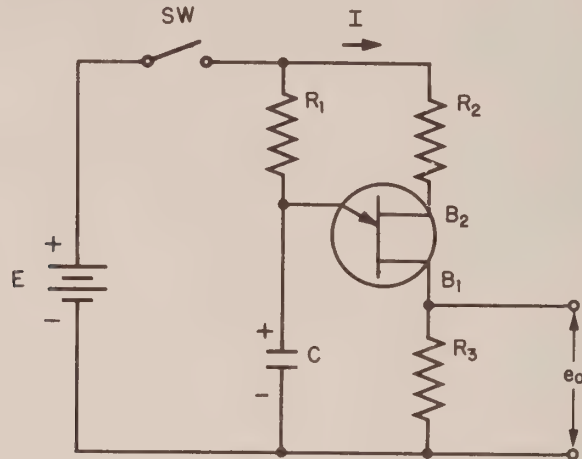


FIG. 10-15 Time-Delay Circuit

When the device triggers or “fires,” the voltage across R_3 increases from the value IR_3 to almost the peak capacitor voltage, after which it decays along an RC discharge curve. It is important to note that the pulse of current through R_3 comes from the capacitor by way of the emitter and does not conduct through resistor R_2 (although the R_2 current is modulated by the emitter current). Resistor R_2 is not necessary for operation but is sometimes included for temperature stabilization.

If the switch remains closed, the device free-runs and generates a series of pulses. However, if the initial capacitor voltage is zero, the first period is longer than subsequent ones because the emitter voltage does not go to zero volts, and the capacitor, therefore, is not completely discharged.

Time delays can also be achieved by counting down from any oscillator or frequency source. Ordinarily the oscillator or frequency source is active all the time, and the divider chain is uncaged or allowed to count at some specific time (t_0). There is, then, a time delay before a divider output signal occurs. This method allows precise time delays since the frequency source may be quite stable. Also, long time delays are possible because the division ratio can be made quite high. A disadvantage is the large number of parts required.

10-6 DESIGN EXAMPLE

A method is to be proposed for implementing a sequencer or serial programmer. The system requirements are as follows:

Unit operation is to be from a single 20-V supply, and a mechanical switching operation is to start after the reception of an uncage signal and proceed automatically thereafter to the conclusion of the program. In particular, the switching operation requires the use of a single-pole, six-position switch which is to be switched sequentially from position 1 to position 6. Initially the switch is in position 1. Upon reception of the uncage or start signal, the device is to switch immediately (less than 0.2 sec) to the number 2 position where it is to remain for 5 sec. At the end of the 5-sec delay, the device should switch automatically to the number 3 position where it should remain for 10 sec. The required time in each position is noted in the following table:

Position	Time Interval (Seconds)
1	--
2	5
3	10
4	20
5	2
6	∞

A number of different techniques can be proposed as solutions to this assignment. However, the mechanical switching requirement suggests the use of a relay tree or a stepping switch somewhere in the design. Stepping switches are available with multiple decks (i.e., poles) and positions in excess of 6. Thus, additional decks would be available for controlling automatic operation of the sequencer.

Stepping switches are electromechanical devices which contain a coil for electromagnetic actuation. Typically, this coil requires a current pulse of approximately 50 mA for at least 50 ms before the wiper or pole advances to the next position. The new position is maintained until the next current pulse occurs.

It would appear that the specified assignment could be satisfied with a certain combination of building blocks which have been described in this chapter. These include the astable, bistable, and monostable multivibrators. The astable type would be used for frequency generation, the bistable for countdown, and the monostable for generation of the necessary stepping switch drive signal. The proposed system is depicted in Fig. 10-16.

Time delay is varied from position to position by varying the frequency of the astable multivibrator (which could be similar to the one depicted in Fig. 10-8). The proposed method varies

frequency by switching to resistors of different values (R_1 , R_2 , R_3 , etc.). Although both timing resistors, 100 k Ω in Fig. 10-8, could be switched, it is not necessary since symmetry is not a requirement.

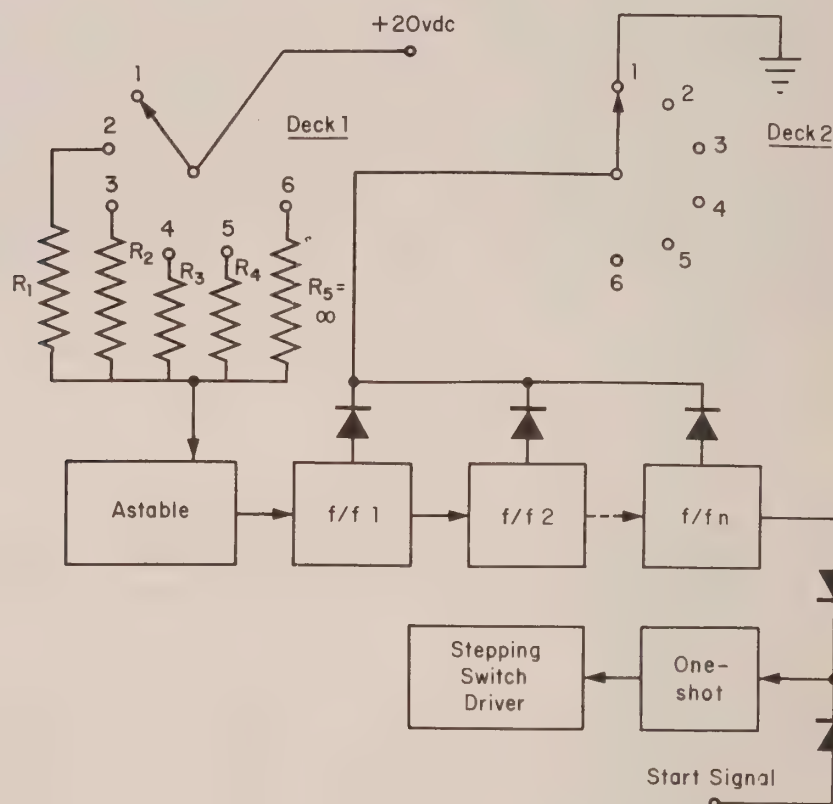


FIG. 10-16 Sequencer

The flip-flops could be similar to the type depicted in Fig. 10-10. The quantity used would depend upon the lowest frequency which one desired to operate the astable device. One combination might be four flip-flops and a maximum astable period of one or two seconds.

Note that the counter is set to the 0 state in position 1 by deck 2 of the stepping switch. There is a time delay from the occurrence of a start signal and an output from the last flip-flop.

The oneshot multivibrator could be similar to that depicted in Fig. 10-6, and the period would be set at approximately 100 ms (something in excess of 50 ms).

Operation is described as follows: An input (uncage) signal triggers the oneshot whose output signal is amplified and applied to the stepping-switch coil. The stepping switch then advances to position 2, the counter is uncaged, and the astable starts operating with a period dependent upon resistor R_1 . After five seconds of time delay, a counter output occurs which triggers the oneshot, the stepping switch advances to position 3, etc.

I am moved to offer one last bit of advice: When confronted by a complex, malfunctioning system, separate the problems insofar as possible, and solve them one by one. I might even say, "Divide and Conquer." Also, good luck.

PROBLEMS

10-1 In the circuit of Fig. 10-1, the input signal is a 10-kc square wave with an amplitude of 10 V peak to peak. The capacitor is $50\ \mu\text{F}$ in value, and the load resistance is $1\ \text{k}\Omega$. What is the equation of the current through R_L if the rectifier is ideal? What is the average current through R_L ?

10-2 A transistor-inverter stage is depicted in Fig. 1.

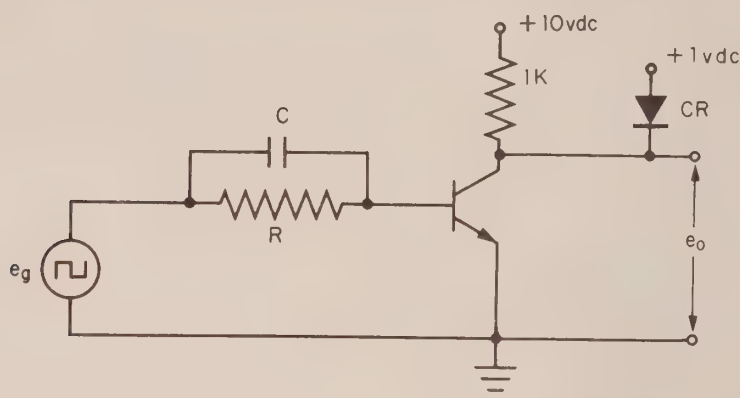


FIG. 1 Inverter

Transistor parameters are specified as follows:

$$h_{FE} = 100$$

$$h_{ie} = 5\ \text{k}\Omega$$

$$C_e = 100\ \text{pF}$$

The input signal is a 10-kc square wave which is equal to $\pm 2\ \text{V}$ in amplitude. Assume that the forward-biased emitter-base voltage is 0 and that the rectifier is ideal.

- Specify a value for resistor R which will cause the collector voltage to swing from $+10\ \text{V}$ to $+1\ \text{V}$.
- Specify a value for RC .
- What would be the peak collector current if R is equal to $10\ \text{k}\Omega$?

10-3 In the circuit of Fig. 10-6, R_3 is $10\ \text{k}\Omega$, C is $0.01\ \mu\text{F}$, R_B is $100\ \text{k}\Omega$, and E is $+15\ \text{Vdc}$.

- What is the oneshot period?
- What is the rise time of the signal at the collector of Q_1 ?
- What is the rise time of the signal at the collector of Q_2 ?

10-4 A free-running multivibrator is depicted in Fig. 2. Transistor current gain is 100, collector-to-emitter voltage rating is 30 V (V_{EC}), and reverse emitter-base voltage rating is 5 V.

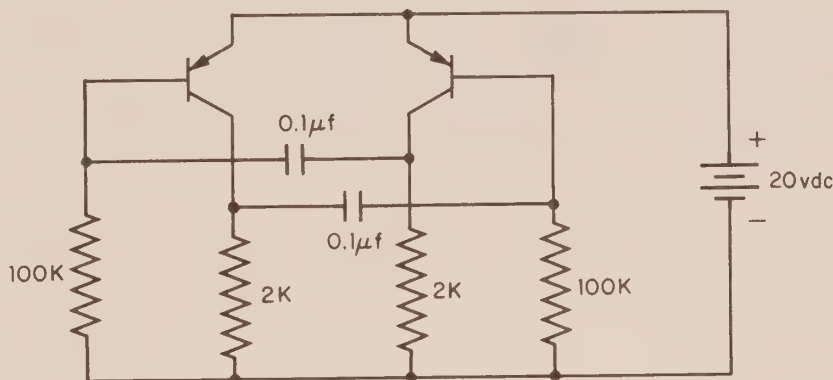


FIG. 2 Astable Multivibrator

- The circuit will not function correctly. Why?
- What would be the operating frequency if correct operation is assumed?
- What are the rise and fall times of the signal at either collector?

10-5 If the output signal from a signal-stage transistor amplifier is to be a fast positive-going waveform, with little or no emphasis on the negative-going edge, what type amplifier and/or connection should be used if large signal operation is assumed. Why?

10-6 A time-delay circuit, of the type depicted in Fig. 10-15, is to be designed to generate a 30-sec delay after closure of the switch. Certain parameters are given as follows:

$$R_{BB} = 7.5 \text{ k}\Omega$$

$$R_3 = 1 \text{ k}\Omega$$

$$\eta = 0.6$$

$$E = 20 \text{ V}$$

Specify values for R_1 , R_2 , and C .

- 10-7 Determine the operating frequency of the circuit depicted in Fig. 3. Assume for all transistors that leakage current, saturation voltage, and forward base-emitter voltage are 0. Also assume correct device operation.

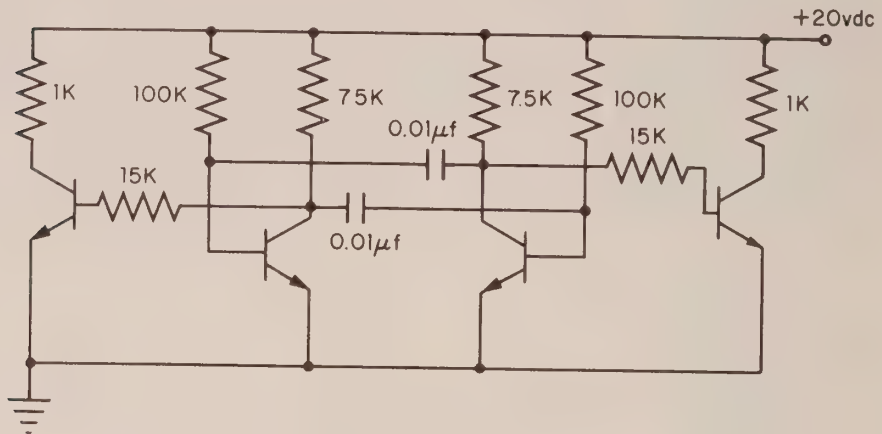


FIG. 3 Astable Problem

- 10-8 Propose a method for implementing an electronic tachometer. The input signal is a voltage pulse of variable amplitude and duration which occurs once per revolution, and the desired output signal is a dc voltage the amplitude of which is directly proportional to the number of revolutions per minute. The dynamic range is 0 to 3,600 rev/min.

PROBLEM ANSWERS

- 1-1 a. 0.25 ampere
b. 2.5 joules
c. 1.25 joules

1-2 0.38 mA

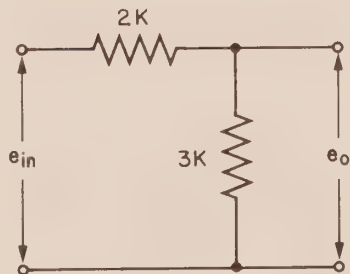
1-3 0.38 mA

1-4 44.7 volts

- 1-5 a. $I = 7$ amperes
 $R = 1.2$ ohms
b. $E = 8.4$ volts
 $R = 1.2$ ohms
c. $I_{sc} = 7$ amperes
 $E_{op} = 8.4$ volts

- 1-6 a. 200 volts
b. 250 volts
c. No

1-7



1-8 One acceptable answer:

$$E = 116 \text{ volts}$$

$$R_1 = 100 \text{ k}\Omega$$

$$R_2 = 100 \text{ k}\Omega$$

$$C = 10 \text{ }\mu\text{F}$$

- 2-1 a. 115 volts
b. 132 watts
c. 60 cps

- 2-2 a. $-\pi/4$ or $-3\pi/4$
b. 400 cps
c. 2.5 ms

- 2-3 a. 50 vdc
b. 70.7 vrms
c. 1,000 pps

- 2-4 a. $\pi/4$ or 45°
b. 354 watts
c. 500 VA
d. $p = 500 [\cos(-\pi/4) - \cos(2\omega t + \pi/4)] \text{ VA}$

2-5 $e = 2E_m/\pi (1 + 2/3 \cos 2\omega t - 2/15 \cos 4\omega t + \dots) \text{ volts}$

2-6 Consider the results of Prob. 2-5.

2-7 One acceptable answer:

$$C_1 = C_2 = 0.1 \text{ }\mu\text{F}$$

$$L_1 = L_2 = 250 \text{ mH}$$

The rms output voltage equals $10/\pi$ volts at a frequency of 1,000 cps.

2-8 One acceptable answer:

Transformer with a turns ratio of 1:2 and connected phase inverting.

3-1 $R = 13 \text{ k}\Omega$
 $C = 0.03 \text{ }\mu\text{F}$

3-2 19.8 watts

3-3 $0.707/\underline{45^\circ}$

3-4 26.6° , 57.6 watts

- 3-5 a. $i = 0.124 + j.124 = 0.175 / \underline{45^\circ}$ amperes
 b. $P = 3.06$ watts
 c. Single signal with a 45° phase angle with respect to the zero phase signal.

3-6 $-j 104$ ohms

3-7 $RC \geq 0.66$
 Capacitor voltage rating > 110 volts
 One acceptable answer:

$$R = 15 \text{ k}\Omega$$

$$C = 50 \text{ }\mu\text{F}$$

3-8 Assuming $C_1 = C_2 = C_3$:

$$E_o/E_{in} = \frac{-R_1 R_2 R_3}{|X|^2 (2R_1 + 2R_2 + R_3) - R_1 R_2 R_3}$$

$$f_o = \frac{1}{2\pi C \sqrt{3R_1 R_2 + 2R_1 R_3 + R_2 R_3}}$$

One acceptable answer:

$$C_1 = C_2 = C_3 = 0.1 \text{ }\mu\text{F}$$

$$R_1 = 1.5 \text{ k}\Omega$$

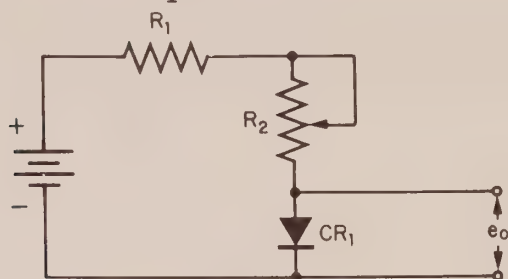
$$R_2 = 1.6 \text{ k}\Omega$$

$$R_3 = 1.8 \text{ k}\Omega$$

$$E_o/E_{in} = -.035$$

Nominal $f_o \cong 404$ cps

4-1 One acceptable answer:



$$R_1 = 5.1K \pm 5\%, \frac{1}{4}W, \text{ Composition}$$

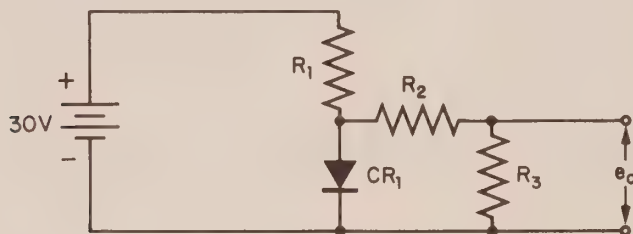
$$R_2 = 20K \pm 10\%, \frac{1}{2}W, \text{ Carbon Potentiometer}$$

$$CR_1 = \text{Silicon General Purpose (1N645)}$$

4-2 a. 29.4 volts
b. 25 volts

4-3 Approximately 1.5 volts

4-4 One acceptable answer:

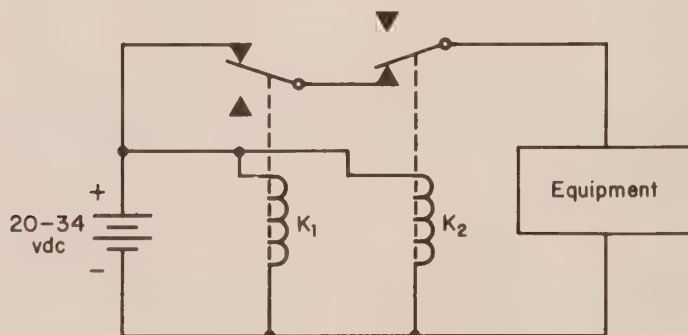


$$R_1 = 30K \pm 5\%, \frac{1}{4}W, \text{ Composition}$$

$$R_2 = R_3 = 20K \pm 1\%, \frac{1}{4}W, \text{ Metal Film}$$

$$CR_1 = \text{Silicon General Purpose (1N645)}$$

4-5 One acceptable answer:



Relays K_1 and K_2 are of the momentary type with K_2 shown in the energized state.

K_1 —SPDT, 5-A contact rating

Pull-in voltage 34 V

K_2 —SPDT, 5-A contact rating

Dropout voltage 20 V

4-6 One acceptable answer:

Inductor— $1\text{H} \pm 5\%$, current rating .5 A

DCR 10 ohms

Capacitor— $22\text{ }\mu\text{F} \pm 10\%$, 35 V, Tantalum

4-7 One acceptable answer:

$R = 200\text{ K} \pm 1\%$, $\frac{1}{4}\text{W}$, metal film

$C = 0.5\text{ }\mu\text{F} \pm 3\%$, 50 V, polystyrene

5-1 a. -20

b. $6.67\text{ k}\Omega$

c. -6.5

5-2 a. $2.6\text{ k}\Omega$

b. -290

c. -114

d. $C_1 = 2.2\text{ }\mu\text{F}$ ($2.15\text{ }\mu\text{F}$ minimum)

$C_2 = 0.47\text{ }\mu\text{F}$ ($0.455\text{ }\mu\text{F}$ minimum)

5-3 a. $2.7\text{ k}\Omega$ (approx.)

b. 2 kc (approx.)

5-4 100 kc (approx.)

$$5-5 \quad A_v \cong \frac{-(h_{fe})(R + jX_L)}{R_g + R_{in}}$$

5-6 a. $13.2 \angle 180^\circ$, 1.3 volts

b. $6.5 \angle 140^\circ$ (approx.)

5-7 One acceptable answer:

Transformer with a 1:3 turns ratio and connected phase inverting.

5-8 One acceptable answer:

$$R_1 = 3 \text{ k}\Omega$$

$$R_2 = 5 \text{ K potentiometer set at approximately } 4 \text{ k}\Omega$$

$$R_3 = 130 \text{ }\Omega$$

$$C_1 = C_2 = 0.1 \text{ }\mu\text{F}$$

6-1 $14.8 - j35.5 = 38.5 \angle -67.4^\circ$

6-2 a. 0.5 watts

b. 20 volts

c. 100 mA

6-3 Approximately 20 sq in.

6-4 a. 102 μA

b. 400 mV

6-5 0.08 μF , 0.1 μF

6-6 Connect a capacitor, approximate value of 300 picofarads across the output.

6-7 a. Collector diode breakdown but probably not transistor destruction.

b. Emitter-base diode destruction from excessive forward current.

6-8 Acceptable values:

$$R_1 = 5.1 \text{ K}, 10 \text{ K maximum}$$

$$R_2 = 124 \text{ K}$$

$$C_1 = 0.1 \text{ }\mu\text{F}, 0.004 \text{ }\mu\text{F minimum}$$

$$C_2 = 0.001 \text{ }\mu\text{F}$$

$$V_{CE} = 22 \text{ volts peak}$$

$$I_C = 100 \text{ mA when discharging } C_2 (\beta \text{ limited})$$

7-1 a. 300 $\text{k}\Omega$

b. 17 (approx.)

c. 3.6 $\text{k}\Omega$

d. 16 $\text{k}\Omega$

e. 10 μF

- 7-2 a. $1.8 \text{ M}\Omega$
 b. 48
 c. 8.4 vdc
- 7-3 a. $R_1 = 18 \text{ k}\Omega$
 $R_2 = 22 \text{ k}\Omega$
 b. $7.9 \text{ k}\Omega$
 c. 0.25
- 7-4 One acceptable answer:
 Emitter follower with a 10-K dc load resistor and two $21 \text{ K} \pm 1\%$ base-biasing resistors.
- 7-5 a. Sinusoidal signal, half-wave rectified.
 b.
 $(A E_m / \pi)(\pi/2 \cdot \cos \omega t + 2/3 \cdot \cos 2\omega t - 2/15 \cdot \cos 4\omega t + \dots)$
- 7-6 a. Approximately 5 volts
 b. $10.8 \text{ k}\Omega$
 c. 28
 d. Approximately 13 volts
- 8-1 $A = -100$
- 8-2 a. $R_{in} = (10)^5 / (n_1 n_2)^2 \text{ ohms}$
 b. 40 dB
 c. 56%
 d. 0
- 8-3 $1.4 \text{ k}\Omega$
- 8-4 a. $2 \text{ k}\Omega$
 b. $1 \text{ k}\Omega$
- 8-5 a. $-1.3 \times 10^5 (K_1 = -12, K_2 = -59, K_3 = -184)$
 b. -100
- 8-6 a. -9.4
 b. -7.5
 c. -8.5 (Experimental)
- 8-7 No definite answer since generator and load impedances are not specified. Possible answers: Two common-emitter amplifiers, one common-emitter amplifier and transformer, one common-base amplifier.

8-8 One acceptable answer:

$$R_1 = 430 \, \Omega$$

$$R_2 = 150 \, \text{k}\Omega$$

$$C_3 = 0.001 \, \mu\text{F}$$

- 9-1 a. 1.07 volts peak
b. 0
c. 2.14 volts peak

$$9-2 \quad \frac{e_o}{e_{in}} = \frac{-(j\omega)(15 \times 10^{-3})}{1 + (j\omega)(10^{-3})} ; \text{yes}$$

9-3 350 kc

9-4 Down 40 dB

9-5 One acceptable answer:

Z_{in} — 130 K resistor

Z_f — 130 K resistor in parallel
with a $1 \mu\text{F}$ capacitor

A — Infinite

- 9-6 One acceptable answer:
Operational amplifier with two input resistors (R_1 and R_2)
and one feedback resistor (R_f).

$$R_f/R_1 = 5$$

$$R_f/R_2 = 10$$

- 9-7 a. $e(t) = 1 - e^{-t/0.13}$ volts

$$e = 0.63 \text{ volt at } t = 0.13 \text{ sec}$$

- b. $e(t) = -t/RC$ volts

$$e = -1.0 \text{ volt at } t = 0.13 \text{ sec}$$

$$e = -2.0 \text{ volts at } t = 0.26 \text{ sec}$$

- 9-8 a. Gain-bandwidth/stage = 25 mc
b. Use transistors with $f_\beta > 5 \text{ mc}$; $f_t \cong \beta_o f_\beta$

Where β_o is low-frequency current gain and f_β is the β cutoff frequency. (Effect of negative feedback, i.e., of gain stabilization on bandwidth, not considered.)

- 9-9 a. $A = -250$
b. $\beta = 49/250$
- 10-1 $i_L = 10 \text{ mA}$ for $\pi > \omega t > 0$
 $= 0 \text{ mA}$ for $2\pi > \omega t > \pi$
 $I_{av} = 5 \text{ mA}$
- 10-2 a. Acceptable answer: $20 \text{ k}\Omega$
b. $1 \mu\text{s}$ ($0.5 \mu\text{s}$ minimum)
c. 20 mA for R equals 20 K and C equals zero μF .
- 10-3 a. Approximately 0.73 ms
b. 0.22 ms
c. Insufficient data given to determine rise time, but it is essentially zero compared to 0.22 ms .
- 10-4 a. Peak voltage at either base tends to be essentially $+40 \text{ volts}$ which would cause reverse voltage breakdown of the emitter-base diode and probably also the collector-base diode.
b. Approximately 70 cps .
c. Insufficient data to determine rise time but very fast compared to fall time which is 0.44 ms .
- 10-5 NPN emitter follower or PNP inverter because large-signal, low-output impedance is obtained for positive-going signals.
- 10-6 Acceptable answer:
 $(RC \cong 29)$
 $R_2 = 0$
 $R_1 = 620 \text{ k}\Omega$
 $C = 47 \mu\text{F}$
- 10-7 980 cps

- 10-8 One method: Let the input signal trigger a oneshot multivibrator the output of which is a pulse of fixed amplitude and duration. Then filter the resultant pulse train to obtain the dc average.

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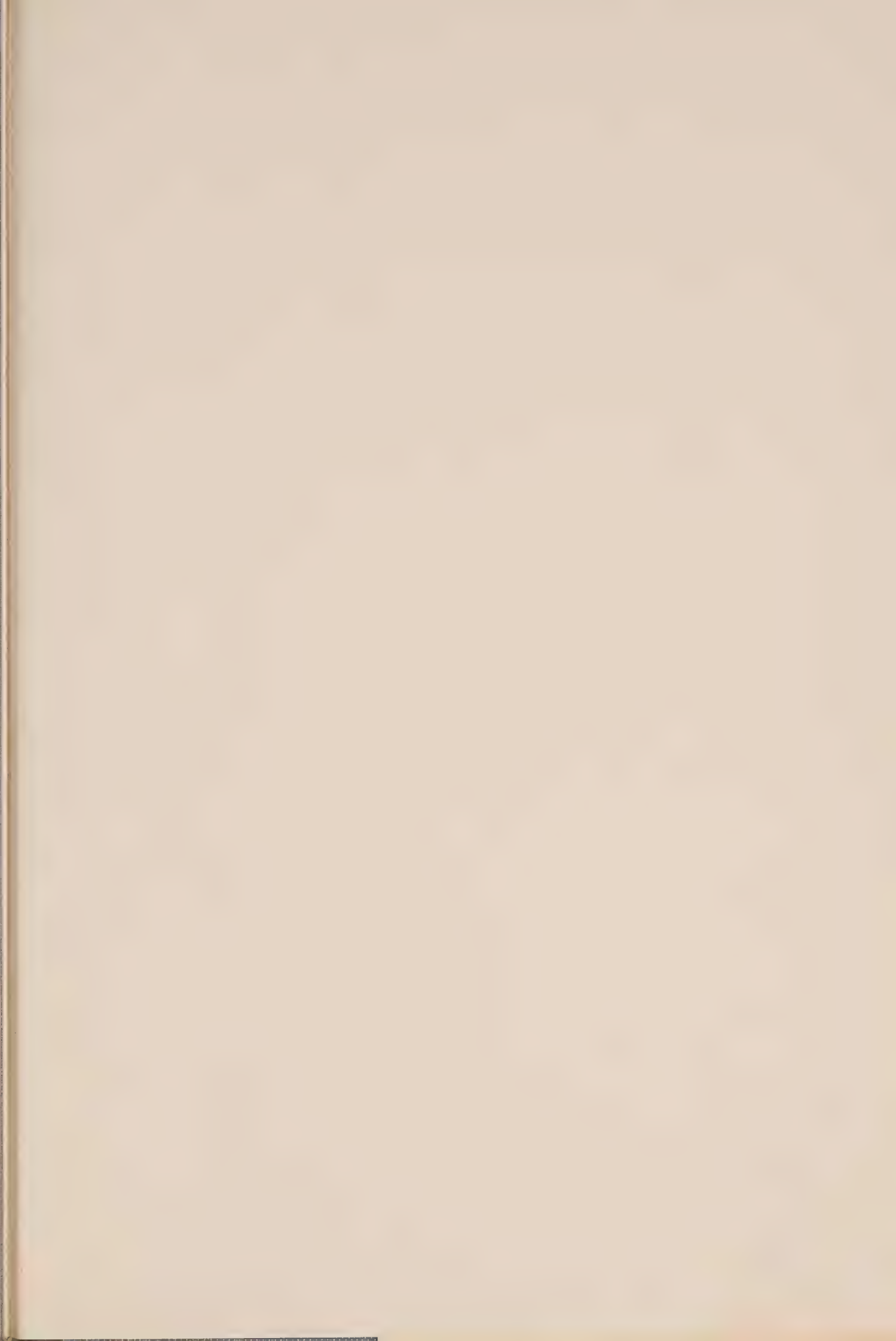
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James D. Long received his BSEE from San Jose State College, and his MSEE from UCLA. Over the past fourteen years he has obtained experience in both the aerospace and electronics areas. Mr. Long's specialty is in solid-state circuit design. However, his work has also entailed circuit development in such systems as early warning radar, air traffic control, radar beacon and altimeter, digital data handling, missile, attitude control, satellite, and frequency generation. In 1957 he designed a transistor time delay circuit which was marketed by the Wheaton Engineering Corporation. Presently, he is employed by the General Technology Corporation where he is Chief Engineer responsible for the engineering and drafting departments. Active as a consultant, he has published numerous articles in his field.

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